Skyechip

Skye's the Limit, Clear Sky Ahead

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SkyeChip, set for listing on the MAIN Market on 20th May 2026, is a Malaysia-based IC design company specializing in standard and custom silicon IP as well as custom ASICs, providing licensable IP for integration and tailored chips for specific customer applications. At the IPO price of RM0.88, Skyechip's stock implies a ~28% discount to both regional and local peers, and we view this stock as one of the proxies to Malaysia's vision to move up the semiconductor value chain. Notably, SkyeChip targets the ex-hyperscaler market — including AI startups, enterprise edge computing players, and companies across various industries that require high-performance, customized chips but lack in-house silicon design teams. As chip designs in these areas become more complex, more companies are turning to external partners for chip design and IP support, indirectly benefiting SkyeChip. We forecast revenue/PAT growth of 32%/30% in FY26 and 30%/32% in FY27, respectively.

Riding the wave of customized chip design. The global semiconductor market is undergoing an irreversible shift towards application-specific, customer-tailored IC solutions, driven by the demand for chips optimized for power efficiency, performance, integration, and footprint, as off-the-shelf solutions often cannot meet the unique requirements of modern AI, HPC, automotive, and edge-computing applications. Rising chip design complexity and costs are also driving more companies to outsource semiconductor design and IP development, benefiting specialized design houses such as SkyeChip. Our deep dive reveals that SkyeChip is uniquely positioned to capitalise on this trend, differentiated by its more comprehensive and higher-end IP portfolio spanning current- to next-generation technologies. Its offerings include advanced memory interface IPs (HBM3/HBM3e, DDR4/5, LPDDR4/5, and in-progress HBM4/LPDDR6), NoC IP, D2D and UCIe interfaces, as well as custom ASIC capabilities, enabling customers to deploy high-performance, scalable solutions with lower integration risks and faster time-to-market. Capitalizing on this rising demand for tailored chip designs translates into a sustainable growth engine for the company.

Modular and scalable business model. SkyeChip's business is built for flexible, repeatable growth, leveraging a modular approach where its silicon IPs and custom ASIC designs can be adapted across multiple projects and applications with minimal modification. We note that customer stickiness is high, as subsequent generations of products are likely to reuse IP blocks from the same vendor, reinforcing long-term relationships and recurring revenue. While its current revenue is mainly driven by project-based engineering fees and IP licensing, we see the potential for it to evolve towards a royalty-based model tied to customers' mass production volumes, which would provide a more recurring and scalable revenue stream.

Access to advanced technologies from top global foundries. SkyeChip has secured access to process design kits (PDKs) from multiple leading foundries, enabling IC and silicon IP design down to 3nm process nodes. These PDKs provide critical design rules, simulation models, and documentation to ensure manufacturability, yield, and compliance with foundry requirements. Complemented by specialized EDA tools and Verification IPs from third-party providers, these capabilities allow SkyeChip to develop high-performance, reliable, and manufacturable semiconductor solutions, reinforcing its technological leadership and supporting scalable growth across a

OUTPERFORM

IPO Price: **RM0.88**
Fair Value: **RM2.00**

Share Price Performance	
KLCI	1,740.22
YTD KLCI chg	3.6%

Post-IPO Major Shareholders	
Dato' Fong Swee Kiang	24.0%
Teh Chee Hak	24.0%

IPO proceeds (RM m)	
R&D of IC products	155.1
R&D of silicon IP	56.4
Expansion of operational facilities	19.0
Expansion of computing infra and labs	38.1
Subscription, licensing and other tools	36.7
Working capital	32.4
IPO expenses	14.3
Total	**352.0**

Summary of IPO	
Enlarged Share Cap (m)	1,796
IPO Price (RM)	0.88
Market Cap Upon Listing (RM m)	1,580
Shariah Complaint	Yes

Summary Earnings Table

FYE May (RM m)	2025A	2026F	2027F
Turnover	119.5	158.1	205.5
EBIT	36.5	48.8	64.5
PBT	37.0	49.2	64.9
Net Profit	35.9	46.7	61.7
Core Net Profit	35.9	46.7	61.7
Core EPS (sen)	2.0	2.6	3.4
Core EPS Growth (%)	6.6	29.9	32.0
NDPS (sen)	0.7	0.7	0.9
BVPS (RM)	0.1	0.1	0.3
Core PER (x)	44.0	33.8	25.6
PBV (x)	12.5	9.4	2.9
Net Gearing (x)	-	-	-
Net Div. Yield (%)	0.8	0.7	1.0

diverse customer base. We opine that having access to PDKs from top global foundries is a testament to SkyeChip's technical capability, serving as the essential "admission ticket" to participate in high-end chips, including AI and other advanced semiconductor applications.

Initiate with an OUTPERFORM call. We assign a TP of RM2.00 to SkyeChip, based on 50x CY27F EPS, representing a ~28% discount to both regional and local peers in the IC design industry. We view the valuation as justified, as SkyeChip is one of the few listed IC design companies that aligns with Malaysia's vision to move up the semiconductor value chain, possesses the technical capability to match regional peers, and is well-positioned to benefit from rising demand for custom chips across various applications. As the company continues to demonstrate strong execution and expand its IP portfolio, successful project delivery and earnings growth should support and justify this valuation over the coming years. Our TP also includes a -3% discount to reflect a 2.5-star ESG rating as appraised by us (see Page 14).

Key risks include: (i) key man risk, where the company's reliance on its senior management team could affect strategy execution if disrupted, **(ii) innovation risk**, as failure to develop advanced IP or keep pace with evolving semiconductor and custom ASIC trends may limit competitiveness, and **(iii) project execution risk**, since revenue is largely derived from milestone-based contracts, introducing potential modelling uncertainty and timing variability in revenue recognition.

Company Overview

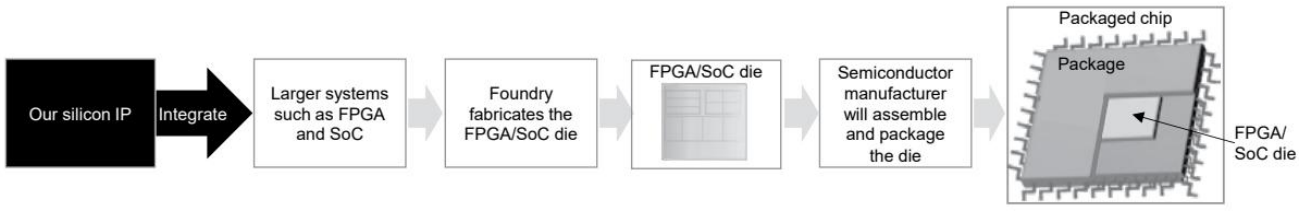
SkyeChip is an original IC design company principally involved in silicon IP and silicon product development, including standard silicon IP, custom silicon IP and custom ASIC solutions. The company provides licensable silicon IPs that customers integrate into their own IC products, while also designing application-specific chips tailored to individual customer requirements. Its business is positioned around specialised semiconductor design rather than general-purpose chip manufacturing, with a focus on performance optimisation, power efficiency, compatibility with industry standards and customer-specific functionality. As an IP-owning design house, SkyeChip retains intellectual property rights over its designs, supported by 36 registered patents across Malaysia, China and the USA, with a further 77 patents pending.

Company is seeking to IPO on 20th May 2026 at the MAIN market, involving an offer for sale new shares of 400m, with the enlarged share base giving Skyechip a potential market capitalization of RM1.58b based on the offer price. Post IPO, Skyechip's key shareholders are expected to be Dato' Fong Swee Kiang (24.0%) and Teh Chee Hak (24.0%)

Skyechip operates across two key segments

- **Silicon IP Design**
    - **Standard Silicon IP**: SkyeChip provides licensable standard silicon IPs that are integrated into customers' IC products. These IPs are developed in accordance with recognised industry standards, such as JEDEC's HBM3 and HBM3E standards, as well as UCIe die-to-die interconnect specifications. This allows SkyeChip's IPs to be compatible with a wide range of customer products, memory suppliers and semiconductor ecosystems. The segment supports customers that require proven, standardised IP blocks to accelerate their IC product development while reducing design complexity and time-to-market.
    - **Custom Silicon IP**: SkyeChip also develops custom silicon IPs based on individual customer specifications and technical requirements. Unlike standard silicon IPs, these solutions are tailored to suit the customer's specific product architecture, performance needs and interface requirements. The company's custom silicon IPs include multi-interface protocol IPs that support various standards and communication protocols, such as DDR, LPDDR, MIPI, LVDS and multi-standard I/O interfaces. This segment contributed 55.4%, 36.6%, 9.2% and 11.1% of total revenue for FY23, FY24, FY25 and FPE October 2025 respectively.
- **Custom ASIC**: SkyeChip expanded into the design and development of custom ASIC products in September 2023. Custom ASICs are semiconductor chips designed for specific applications rather than general-purpose use, allowing customers to achieve stronger performance, better power efficiency and a smaller physical footprint. This segment enables SkyeChip to deliver highly tailored chip solutions that can support proprietary algorithms and specialised functions that standard devices may not handle efficiently. Custom ASICs also provide stronger IP protection, as key functionality is embedded directly at the hardware level.

Exhibit 1: Skyechip's Position within the Value Chain of Producing a Chip



Source: Company Report, Kenanga Research

Key Management

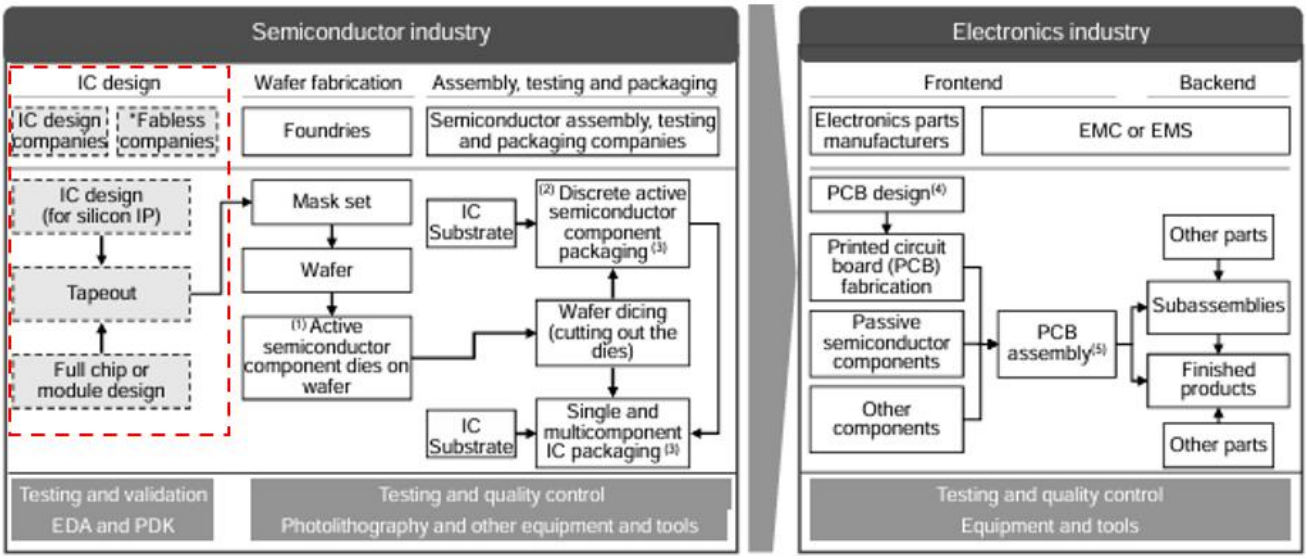
1. **Dato' Fong Swee Kiang (Chief Executive Officer)** is SkyeChip's Non-Independent Executive Director and Chief Executive Officer, appointed on 17 September 2019. He holds a Bachelor of Electrical Engineering with first-class honours from Universiti Teknologi Malaysia (1986) and an MBA from Washington University in St. Louis (2010), and was conferred the Darjah Setia Pangkuan Negeri (D.S.P.N) in 2025. With over 35 years in the semiconductor industry, he began his career at Intel, rising to Director of the Penang Design Center, and later held senior roles at Altera Malaysia and Avago Technologies (Broadcom), leading engineering, R&D, and global operations. Since joining SkyeChip in 2019, he has overseen the company's strategy, operations, sales, and marketing, guiding the executive team, driving innovation, fostering growth, managing risks, and ensuring effective governance.

2. **Teh Chee Hak (Chief Technology Officer)** is SkyeChip's Non-Independent Executive Director and Chief Technology Officer, appointed on 5 February 2023. He holds a Bachelor of Engineering (Honours) in Electrical and Electronic Engineering from Universiti Sains Malaysia (2000). He has over 20 years of semiconductor industry experience, having developed deep expertise in processor, memory, I/O, and FPGA architecture through roles at Intel Microelectronics (2000–2012; 2016–2020), where he progressed from engineer to chief architect, including assignments in the USA, and at Altera Malaysia (2012–2016) as principal engineer and architect, responsible for memory interface and FPGA microarchitecture. Since joining SkyeChip, he has served as CTO, overseeing technical strategy and leading the design and development of advanced silicon IPs and custom ASICs for AI and high-performance computing applications, driving innovation across the company's product portfolio.

3. **Galvin Wong (Finance Director)** has over eight years of experience in finance and investments. He is a member of both the Malaysian Institute of Accountants (MIA) and ACCA, and began his career in 2017 at AmFunds Management Bhd in equities research. He subsequently joined Abrdn Islamic Malaysia Sdn Bhd as an investment analyst, where he continued focusing on equities research and was later promoted to investment manager in 2022, expanding his responsibilities into fund management. He joined the Group in 2023 as Strategic Financial Controller and was promoted to Finance Director in October 2025. In his current role, he oversees statutory financial reporting, financial planning, and corporate compliance, while shaping the Group's financial strategy and supporting key financial decisions. He also manages treasury operations including foreign exchange, hedging, cash and liquidity management, and maintains active engagement with external stakeholders such as auditors, investors, and bankers.

Who's Really Behind Every Chip?

Exhibit 2: Semiconductor's Value Chain Analysis



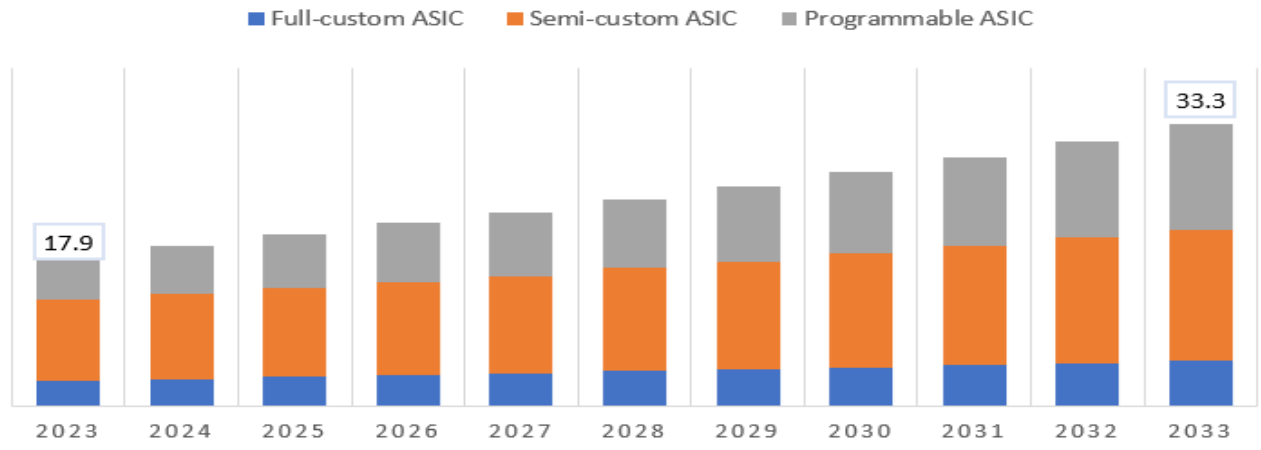
Source: Company Report, Kenanga Research

- **The answer is IC design company,** which sits at the very beginning of the semiconductor value chain, forming the intellectual backbone of all downstream manufacturing and assembly activities. Companies in this segment, often referred to as 'fabless' or silicon IP providers, focus on creating the architecture, logic, and functional design of chips without owning fabrication facilities. Skyechip operates within this IC design layer, specializing in IP development and custom ASIC solutions. Its role is critical: the quality, flexibility, and efficiency of its designs directly influence the performance, manufacturability, and cost-effectiveness of chips produced by wafer fabs, assembly houses, and packaging companies downstream. Skyechip's customer base primarily includes fabless semiconductor companies, system-on-chip (SoC) developers, and electronics manufacturers seeking high-quality IP for integration into their products. By providing modular, licensing-based IP and design solutions, Skyechip enables semiconductor and electronics companies to accelerate development while reducing upfront R&D burden.

What's Shaking Up IC Design's Industry Today?

Rise of AI ASIC application and Outsourcing Supercycle

Exhibit 3: Market Size of Application Specific Integrated Circuit (ASIC) – USDb



Source: Market.US, Kenanga Research

Exhibit 4: Customer-Product Mapping to IC Design Providers (Kenanga Compilation)

Customer	ASIC product	Code Name	IC design	1H25	2H25	1H26	2H26	1H27	2H27	1H28	2H28
	TPU v7	Ironwood	Broadcom								
	TPU v8AX/ v8x	Sunfish	Broadcom, Mediatek								
	TPU v8e/ v8p	Humufish	Mediatek, Broadcom								
	TPU v9p	Icefish	Broadcom								
aws	Trainium 2	-	Marvell								
	Trainium 3	-	Alchip								
	Trainium 4	-	Alchip								
	Maia 200	Braga	GUC								
	Maia 300	Griffin	Marvell								
	MTIA 300	Athena	Broadcom								
	MTIA 400	Iris/Iris+	Broadcom								
	MTIA 450	Arke	-								
	MTIA 500	Astrid	-								
	MTIA 600	Apollo	-								
	Baltra-Sotra	-	Broadcom								
	Titan v1	Nexus	Broadcom								
	Titan v2/v3	-	Broadcom								
	A15	-	GUC								
xAI	X1	-	Broadcom								
SoftBank	Izanagi 1/2	-	Broadcom								

Source: Various news sources, Kenanga Research

- **AI inference economics are driving rapid adoption of custom ASICs.** High GPU costs and the need for energy-efficient inference workloads are pushing hyperscalers to develop chips in-house, but not every company has the resources or expertise to assemble a full silicon team. This creates a structural opportunity for outsourced ASIC implementation partners, positioning them at the centre of the next phase of semiconductor growth. Notably, Skyechip captures the ex-hyperscaler market—AI startups, enterprise edge computing players, and companies in automotive and industrial sectors that require high-performance, customized chips but lack internal silicon teams. Rising tapeout (completed design is sent to the semiconductor foundry for manufacturing) complexity in these segments reflects the growing difficulty of integrating larger, more performance-intensive designs under tighter power, cost, and time-to-market constraints. This increases reliance on external IP and specialist design expertise, providing SkyeChip with indirect but substantial benefits. As shown in the global ASIC market forecast compilation by Kenanga, where the market is expected to grow by a CAGR of 7% over the next seven years to USD33b by 2033 (exhibit 3), this growth is structural rather than a one-off spike, with the emergence of AI simply accelerating an ongoing expansion across full-custom, semi-custom, and programmable ASIC segments.

- **We are already seeing this trend unfold among major players**. From Kenanga's compilation (exhibit 4), we notice that hyperscalers such as Google, Meta, and Amazon are running multi-year ASIC roadmaps with repeat engagements across successive chip generations. This reflects strong IC designer stickiness, where design partners are often retained and carried forward into next-generation chips due to deep platform knowledge and high switching costs. For example, we notice that Amazon's Trainium programs are closely supported by Alchip Technologies, while Google's TPU efforts continue to involve Broadcom. Complex designs from hyperscalers and leading enterprise customers increasingly rely on specialized external teams, creating rising tapeout complexity that Skyechip can leverage. Notably, as Skyechip's IP is integrated into a generation of ASICs, subsequent product iterations are likely to continue using its modular IP blocks, generating repeat demand and strengthening client reliance. Beyond AI, the ASIC design service market is experiencing broad-based growth globally, fuelled by the rising need for customized integrated circuits across automotive, telecommunications, consumer electronics, and industrial automation sectors. Skyechip's licensing-based IP and design capabilities position it to capture incremental value from these expanding opportunities across multiple industries.

AI scaling is increasingly constrained by data movement rather than compute alone

AI scaling is increasingly constrained by data movement rather than compute alone, shifting the focus from raw GPU performance to memory bandwidth, interconnect efficiency, and packaging sophistication. Modern AI silicon can be framed across four layers—compute (GPU scaling), memory (bandwidth and power), interconnect (latency and data movement), and packaging (chiplet and die-to-die integration). Skyechip addresses these bottlenecks through its modular IP and design solutions: its memory IP enables high-bandwidth memory (HBM) integration, its interconnect and fabric architecture IP optimizes latency and data flow between dies, and its expertise in advanced packaging and die-to-die (D2D) integration supports scalable multi-die chiplet designs. These offerings allow hyperscalers, AI accelerator developers, and enterprise ASIC customers to deploy complex architectures efficiently, ensuring workloads scale effectively while minimizing power, latency, and integration challenges.

- **NoC Is a Premium Area**. NoC is now strategic, not commodity. As transistor scaling slows, architectural efficiency drives performance, making sophisticated NoC IP critical for AI accelerators, multi-die chips, HPC, chiplets, and edge AI SoCs. ***Think of it like the highways inside a city: NoC IP is the traffic system connecting all neighbourhoods (dies) efficiently, avoiding congestion.*** Skyechip's NoC interface IP enables low-latency, high-bandwidth communication across dies, supporting scalable multi-die and chiplet architectures.

- **Memory Is the New CPU** Memory bandwidth, hierarchy, and near-memory architectures are the new performance bottlenecks. ***Imagine the brain trying to work but only being able to access a tiny notebook—without memory IP, compute units starve for data.*** Skyechip's memory interface IP optimizes data flow and access efficiency, enabling AI accelerators and complex ASICs to fully utilize compute resources. Companies leveraging high-quality memory and NoC IP can structurally outperform peers, as these interfaces are central to scaling modern AI workloads.

Breaking the Monolithic: The Rise of Chiplet Architecture

Exhibit 5: From Traditional Monolithic Chip Architecture…

Source: Wondeful PCB, Kenanga Research

Exhibit 6: …to Advanced Chiplet-Based Architecture

Source: Wondeful PCB, Kenanga Research

- **From Monolithic to Chiplets.** Traditionally, SoCs were built as monolithic chips, where all cores, accelerators, memory interfaces, and peripherals were integrated on a single die. While being a simplified design, it also created scaling, power, and yield limitations as transistor densities and functional complexity increase. Chiplet-based architectures break the monolithic design into multiple smaller dies—each specialized for a particular function—that can be integrated in 2.5D (side-by-side on an interposer) or 3D (vertically stacked) packages. This approach allows higher yield, flexible scaling, and easier integration of heterogeneous technologies, enabling advanced SoCs to meet increasing performance, power, and area demands while accelerating time-to-market.

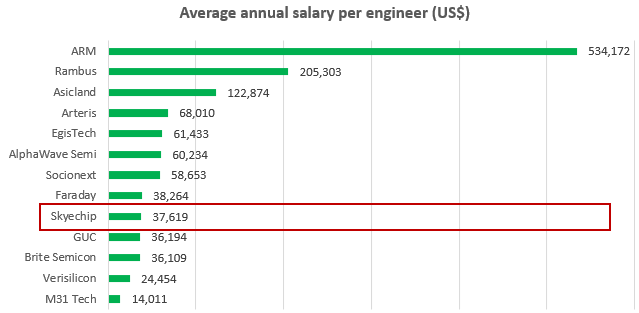
- **Here is where interconnects' role amplifies.** In a chiplet-based system, interconnects are critical for high-speed, low-latency communication between dies. Standards like PCIe and UCIe provide high-speed, low-latency interfaces that connect dies, chiplets, and external components, enabling scalable multi-die designs. Skyechip's NoC and interconnect IP are designed to interface seamlessly with these standards, allowing efficient communication across dies and supporting advanced packaging and chiplet integration.

Why Malaysia for IC Design?

From our channel checks and understanding, we believe there may be curiosity about why product-owning semiconductor and fabless companies would consider Malaysia for IC design services, given the country's traditional reputation as a backend-focused hub rather than a design center.

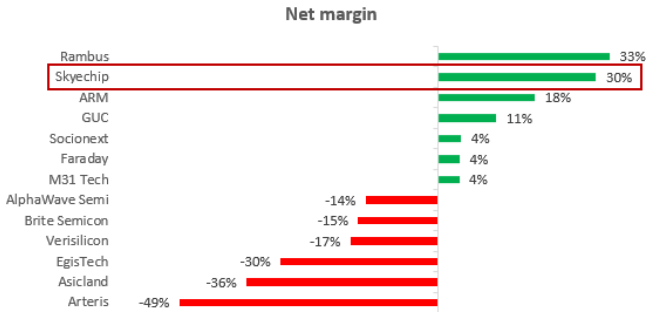
Malaysia Is Emerging as a "Second Node" Engineering Base. We opine that Malaysia won't likely rival Taiwan or the US as the primary semiconductor design hub, but it is increasingly positioned as a secondary engineering node within global ASIC development workflows. Through our discussions with industry participants and institutional investors, we noted growing interest in Malaysia as a cost-competitive, complementary engineering base. Semiconductor firms are actively seeking diversification beyond Taiwan and China due to geopolitical risks, rising wages, talent shortages, and the need to broaden customer and supply chain exposure. In this context, Malaysia's emerging IC design ecosystem—including companies such as Skyechip, Oppstar, Infinecs, Great Asic, and IC Microsystems—enables firms to supplement primary teams, accelerate tapeouts, and scale design capacity efficiently without disrupting established hubs. In this case, we believe that the growth in custom ASIC demand is sufficient to expand the overall market, meaning Malaysia does not need to "take share" from traditional hubs but instead participates in a growing pie.

Exhibit 7: Lower Engineer Costs In Malaysia = More Flexibility for Competitive IC Pricing (USD Per Year)



Source: Kenanga Research

Exhibit 8: Strong Margins Driven By Technical Capability and Cost Control, Not Just Low Labor Costs



Source: Kenanga Research

Cost Advantage Driving IC Design Interest. From a costing perspective, we attempted to identify whether Malaysia has a structural cost advantage in IC design. For IC design companies, we think certain cost components such as EDA tools and software licences are broadly similar across geographies, particularly when companies rely on common vendors such as Synopsys and Cadence. As a result, one of the key differentiating cost components is engineering talent. Based on our data collection and comparison of engineering costs across IC design companies in different countries and regions, Malaysia appears to offer a competitive cost base (exhibit 7). For SkyeChip, the average cost per engineer is approximately USD38,000 per annum, equivalent to around RM13,000 per month, based on the exchange rate assumption used. This is meaningfully lower than selected regional peers such as Socionext, Alphawave, Egis Technology, and Arteris. We believe this lower engineering cost base gives Malaysia, and SkyeChip in particular, greater flexibility in pricing IC design services competitively. This could allow SkyeChip to offer attractive pricing to customers while still preserving profitability, thereby gaining a potential edge over higher-cost peers. Notably, we think SkyeChip's cost competitiveness is unlikely to come at the expense of margins as the company continues to generate one of the stronger margins among its selected peer group (exhibit 8), suggesting that its pricing advantage is more likely driven by structural cost efficiency rather than margin compromise.

Why Skyechip?

Exhibit 9: Most Players Target Similar End Markets…

Company	Memory IPs	NOC	D2D	PCIe/UCIe	Custom ASIC
Skyechip	✓	✓	✓	✓	✓
ARM	✓	✓		✓	
GUC	✓		✓		✓
Rambus	✓			✓	
Faraday	✓			✓	✓
AlphaWave Semi	✓	✓	✓	✓	
Brite Semicon	✓			✓	✓
EgisTech	✓		✓	✓	✓
M31 Tech	✓			✓	✓
Asicland					✓
Quest Global					✓
Socionext	✓			✓	✓
Verisilicon				✓	✓
Arteris		✓			✓

Source: Company, Kenanga Research

Exhibit 10: …But Their IP Portfolios Show Unique Strengths

	IOT	Consumer	Auto	AI
Skyechip	✓	✓	✓	✓
ARM	✓	✓	✓	✓
GUC (Global Unichip)	✓	✓	✓	✓
Rambus	✓	✓	✓	✓
Faraday Technology	✓	✓	✓	✓
AlphaWave Semi	✓	✓	✓	✓
Brite Semicon	✓	✓		
EgisTech		✓	✓	✓
M31 Tech	✓	✓	✓	✓
Asicland	✓		✓	✓
Quest Global			✓	
Socionext	✓		✓	✓
Verisilicon	✓	✓	✓	
Arteris	✓	✓	✓	✓

Source: Company, Kenanga Research

Exhibit 11: Deeper Dives into Their Respective IP Capabilities Reveal The Real Story

Companies	HBM3	HBM3e	HBM4	HBM4e	LPDDR4/4x	LPDDR5/5x	LPDDR6	DDR4	DDR5	PCIe	Ethernet	CXL	SerDes	UCIe/D2D	Coherent NoC	Non-Coherent NoC	MIPI
Skyechip	✓	✓	In-progress		✓	✓	In-progress	✓	✓					✓	✓	✓	✓
ARM										Partial					✓	✓	
GUC (Global Unichip)	✓	✓	✓		✓	✓	✓	✓	✓					✓			✓
Rambus	✓	✓	✓	In-progress	✓	✓	✓	✓	✓	Up to PCIe 7		✓	6-56G	✓			✓
Faraday Technology					✓			✓		Up to PCIe 4	✓		12.5-28G				✓
AlphaWave Semi	✓				✓	✓		✓	✓	✓	✓	✓	1-112G	✓			
Brite Semicon					✓			✓		Up to PCIe 4			2.5-32G				✓
EgisTech					✓	✓		✓	✓					✓			✓
M31 Tech					✓					Up to PCIe 5			5-10G				✓
Asicland																	
Quest Global																	
Socionext										Up to PCIe 4			1G-56G				✓
Verisilicon										Up to PCIe 3.1			1.25-16G				✓
Arteris															✓	✓	
Cadence	✓	✓	✓	In-progress	✓	✓	✓	✓	✓	Up to PCIe 7	✓	✓	Up to 224G	✓			✓
Synopsys	✓	✓	✓	In-progress	✓	✓	✓	✓	✓	Up to PCIe 7	✓	✓		✓			✓

Source: Company Report, Kenanga Research

Broad Memory Ip Coverage Sets Skyechip Apart. Based on the peer comparison (exhibit 11), SkyeChip stands out for having a relatively broad memory IP coverage across both high-bandwidth memory and mainstream/mobile memory standards. It already covers HBM3, HBM3e, LPDDR4/4x, LPDDR5/5x, DDR4 and DDR5, while also showing HBM4 and LPDDR6 as in progress. This is important because many smaller peers appear concentrated in selected memory types or older standards like LPDDR4 and DDR4, whereas SkyeChip is positioned across current and next-generation memory interfaces. The key differentiation is therefore the technology breadth in memory IP, especially its exposure to AI/HPC-related memory demand through the latest HBM generation.

NoC is A Differentiated Offering. One of the more underappreciated aspects of SkyeChip's portfolio is its NoC capability, which positions the company within a much narrower and higher-value segment of the semiconductor IP ecosystem. NoC has become increasingly important in modern AI and high-performance computing architectures because traditional bus-based communication structures are no longer sufficient to efficiently manage the massive data movement requirements within advanced SoCs and chiplet-based systems. As AI accelerators continue scaling in compute density, the key bottleneck is increasingly shifting towards on-chip communication efficiency, memory bandwidth utilisation, latency management, and power-efficient data transfer between compute clusters, memory subsystems, and accelerators. This is where NoC architecture becomes critical, effectively serving as the "traffic management system" inside complex chips.

Strategic Value Lies In the Full IP Portfolio. Evaluating IC design companies requires looking at their IP portfolio holistically. While competitors may target similar markets, SkyeChip's breadth and integration of memory IP, NoC solutions, and emerging interfaces allow it to deliver more complete and high-performance system solutions. This comprehensive portfolio enables customers to adopt SkyeChip IP with fewer compatibility concerns, faster time-to-market, and improved scalability for AI, HPC, and next-generation computing applications. In effect, the company's strategic advantage is not just in individual IP blocks, but in the synergy across its portfolio, which translates into differentiated value for both chip designers and end users.

Investment Merits

1. **Riding on Increasing Demand for Customized Chip Design**

- **The Irreversible Shift Toward Custom Chip Design.** The global semiconductor market is experiencing a pronounced shift toward application-specific and customer-tailored IC solutions, driven by the rapid growth of AI, high-performance computing, mobile devices, consumer electronics, and emerging smart technologies. Broadly, we observed that customers are increasingly seeking designs optimized for power efficiency, integration, and performance, rather than relying on generic off-the-shelf solutions. This trend is spreading beyond the largest players, with small and startup companies also outsourcing chip design to meet their specific requirements. We think SkyeChip's in-house capabilities to develop modular, configurable, and reusable silicon IP allow it to respond efficiently to these diverse and complex demands. Notably, we see this ability could position SkyeChip to capture a growing share of the market, particularly with its broad IP portfolio spanning high-end memory interface IP, NoC IP, D2D interface IP, and custom ASICs—turning the rising demand for tailored chip designs into a sustainable growth engine.
- **Beyond the Usual IPs.** Our deep dive into SkyeChip and its peers reveals that the company stands out for offering some of the latest memory interface IPs, spanning current and next-generation standards including HBM3, HBM3e, DDR4/5, LPDDR4/5, and in-progress HBM4 and LPDDR6, providing broad exposure to AI and HPC memory demand. Its differentiated NoC capabilities further position it within a high-value segment of the semiconductor IP ecosystem, addressing critical on-chip communication, latency, and bandwidth challenges in advanced SoCs and chiplet-based systems. Combined with a comprehensive portfolio that includes D2D and UCIe interfaces, SkyeChip's integrated IP offerings allow customers to deploy high-performance, scalable solutions with fewer compatibility concerns and faster time-to-market, making the company uniquely compelling as a total solution provider.

2. **Modular and Scalable Business Model**

- **Scalable and Reusable IP Portfolio:** Over the years, Skyechip has developed a comprehensive library of standard silicon IPs, including memory interface IP, Network-on-Chip (NoC) IP, and D2D interface IP, all created entirely in-house. These IPs are modular and configurable, enabling them to be licensed either in their standard form or adapted to meet the specific operational requirements of diverse customers across multiple regions. This design approach allows the same IP to be deployed across multiple projects and applications with minimal modification, reducing both development time and resource expenditure. By providing a flexible, reusable, and standards-compliant IP portfolio, the company positions itself to achieve scalable business growth while maintaining consistency and reliability across customer deployments.
- **IP Ownership and Revenue Flexibility:** The company retains full intellectual property rights to its silicon IPs, granting customers rights for project-specific usage only. This strategy ensures continued ownership and control over the technology while simultaneously enabling monetization opportunities if the IP is applied beyond the initially licensed projects. By maintaining IP ownership and providing structured licensing arrangements, the company can capture ongoing revenue streams, reinforce its competitive position, and create long-term business value through strategic IP commercialization.

3. **Access to Advanced Technologies from Top Global Foundries…**

…Down to 3nm Nodes. The company has secured access to process design kits (PDKs) from multiple foundries, including the largest and most advanced foundries globally, enabling IC and silicon IP design down to 3nm process nodes. These PDKs provide critical design rules, simulation models, and documentation that ensure manufacturability, yield, and compliance with foundry requirements. Complementing this, the company utilizes specialized EDA tools and Verification IPs from third-party providers, essential for precise IC design, validation, and verification. Collectively, these capabilities allow the company to develop high-performance, reliable, and manufacturable semiconductor solutions, strengthening its technological leadership and supporting scalable business growth across a diverse customer base.

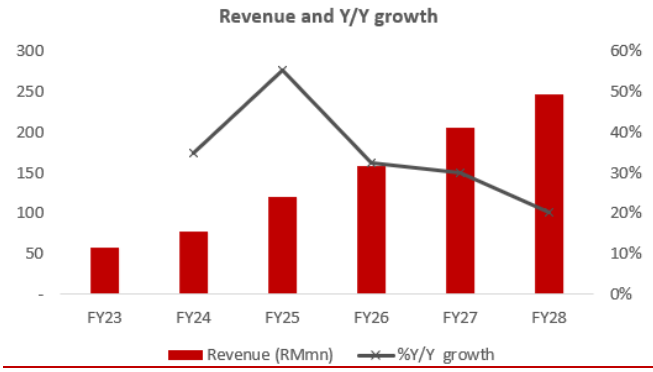
Financial Highlights

Financial review. SkyeChip delivered strong revenue growth over the FYs under review, increasing from RM57.2m in FY23 to RM77.1m in FY24, and further to RM119.5m in FY25, representing a CAGR of 44.6%. The growth was primarily driven by higher demand for standard silicon IP, including memory interface IP and Network-on-Chip IP, as well as the commercialisation and sales of custom ASIC products, including a specialised IoT ASIC for AI edge computing. Revenue from custom silicon IP fluctuated due to project completion cycles but remained a meaningful contributor to total revenue. Notably, GPM decreased from 59.1% in FY23 to 46.8% in FY24 and 42.2% in FY25, largely due to higher design, development, and manufacturing costs. Profit Before Tax (PBT) margin also declined from 49.7% in FY23 to 44.9% in FY24 and 31.0% in FY25,

reflecting increased administrative expenses and lower GP margin. Nevertheless, SkyeChip's strong revenue growth, sustainable profitability, and expanding silicon IP and ASIC portfolio demonstrate its ability to maintain positive operating leverage and financial resilience. On the profitability front, Profit After Tax (PAT) increased from RM28.6m in FY23 to RM33.7m in FY24, and further to RM35.9m in FY25, reflecting strong contributions from both silicon IP and custom ASIC segments. PAT margin declined from 50.1% in FY23 to 43.7% in FY24 and 30.1% in FY25, primarily due to higher technical staff costs, depreciation, and increased spending on semiconductor materials for custom ASIC production. Despite this, the Group maintained healthy absolute profitability, supported by high-margin standard silicon IP projects and the successful rollout of custom ASICs.

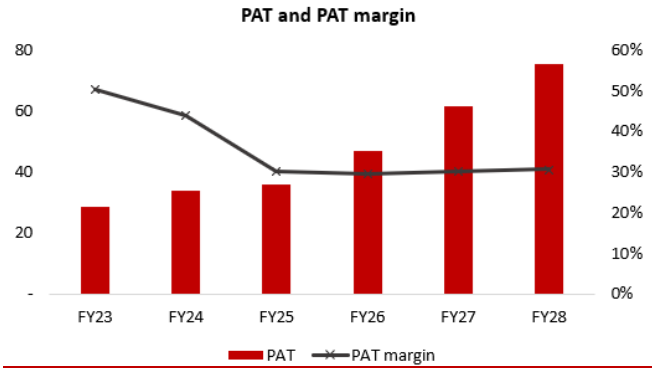
Financial forecasts. We forecast revenue to grow by 32% and 30% YoY in FY26 and FY27, respectively, driven by a strong pipeline from both the silicon IP segment and custom ASIC. Consequently, PAT is projected to grow by 30% and 32% in FY26 and FY27, respectively, with margins expected to remain stable at around 30%. The company does not have a formal dividend payout policy, but it targets a payout ratio of up to 25% of PAT attributable to owners for each financial year. While we see potential for the company to gradually transition towards a royalty-based revenue model, we have not factored any such contribution into our forecasts. This is because the realization of royalty streams is contingent on successful customer onboarding into such structures and the associated commercialization timelines, which remain uncertain at this juncture. Notably, as observed among selected regional peers, revenue derived from royalty and turnkey models can account for approximately 70–80% of total revenue, depending on product lifecycle stage and ramp-up profile.

Exhibit 12: Revenue and Growth



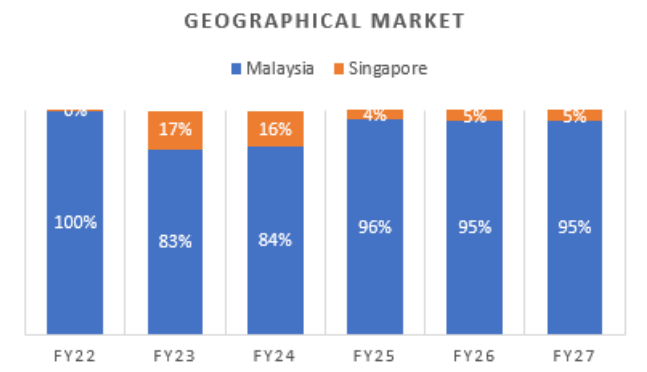
Source: Company, Kenanga Research

Exhibit 13: Net Profit and Margin



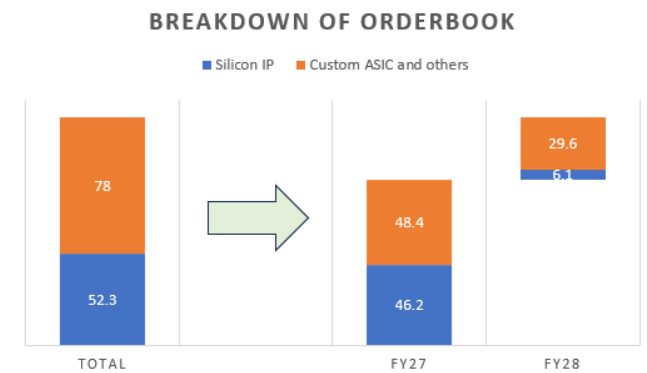
Source: Company, Kenanga Research

Exhibit 14: Skyechip's Geographical Breakdown



Source: Company, Kenanga Research

Exhibit 15: Skyechip's Orderbook Breakdown



Source: Company, Kenanga Research

Valuation

We assign a TP of RM2.00 to Skyechip, based on 50x CY27F EPS, which represents our belief that the stock is worth more than double its IPO offer price. Thjs is because we see valuations as not excessive given an average of 69x PER for its peers (which we included a broad mix of companies from regional peers that develop and commercialise their own IPs, alongside local peers that have historically been more focused on IC design services). Even so, we have applied a discount of c.28% on this valuation to reflect its smaller market capitalization and lower earnings base, which we expect to narrow as it scales and improves profitability. Moreover, Skyechip's technical capability is comparable to regional peers where it is positioned to benefit from rising demand for custom chips across various applications. As the company continues to demonstrate strong execution and expand its IP portfolio, we expect progressive re-rating potential to be driven by sustained earnings growth, successful project delivery, and eventual participation in a royalty-based business model. However, we have not factored in any contribution from royalties into our valuation at this stage, given the uncertainty around customer adoption and commercialization timelines. Our TP also includes a -3% discount to reflect a 2.5-star ESG rating as appraised by us (see Page 14).

Exhibit 16: Comparison of Local And Regional Peers in the Industry

Company	Country	Ticker	Market Cap (RM m)	Revenue (RM m)	Net Margin (%)	1-yr Average Fwd PER (x)
Malaysia						
Oppstar	Malaysia	OPPSTAR MK	503.5	64.0	Loss-making	83.9
Keyasic	Malaysia	KEYA MK	4.1	14.4	Loss-making	N/A
Regional						
ARM	United Kingdom	ARM US Equity	940,612	19,680	18.4	97.7
GUC	Taiwan	3443 TT Equity	86,344	4,394	11.0	111.6
Verisilicon	China	688521 CH Equity	82,420	1,755	Loss-making	475.5 (Outlier)
Rambus	United States	RMBS US Equity	56,456	2,831	32.6	43.5
Socionext	Japan	6526 JT Equity	10,452	4,951	4.3	25.3
Brite Semicon	China	688691 CH Equity	8,236	403	Loss-making	N/A
Arteris	United States	AIP US Equity	6,908	282	Loss-making	N/A
Faraday	Taiwan	3035 TT Equity	6,568	2,316	4.1	43.7
M31 Tech	Taiwan	6643 TT Equity	3,392	229	4.0	79.8
EgisTech	Taiwan	6462 TT Equity	1,524	686	Loss-making	N/A
Asicland	Korea	445090 KS Equity	876	205	Loss-making	N/A
Simple Average			**92,638.1**	**2,908.5**	**12.4**	**69.4**
Skyechip			**1580.5**	**120**	**30%**	**50.0**

Source: Bloomberg, Kenanga Research

Key risks include: (i) key man risk, where the company's reliance on its senior management team could affect strategy execution if disrupted, (ii) innovation risk, as failure to develop advanced IP or keep pace with evolving semiconductor and custom ASIC trends may limit competitiveness, and (iii) project execution risk, since revenue is largely derived from milestone-based contracts, introducing potential modelling uncertainty and timing variability in revenue recognition.

Income Statement

FY Mar (RM m)	2023A	2024A	2025F	2026F	2027F	2028F
Revenue	57.2	77.1	119.5	158.1	205.5	250.7
EBITDA	29.3	32.0	43.4	55.1	71.4	89.2
Depreciation	1.0	1.6	5.1	6.4	6.9	7.6
Operating Profit	28.0	33.6	36.5	48.8	64.5	81.7
Other Income	0.5	6.8	1.6	1.0	1.0	1.5
Interest Exp	0.4	0.9	0.5	0.4	0.4	0.4
PBT	28.4	34.6	37.0	49.2	64.9	82.1
Taxation	0.2	(0.9)	(1.1)	(2.5)	(3.2)	(4.1)
Net Profit	28.6	33.7	35.9	46.7	61.7	78.0

Balance Sheet

FY Mar (RM m)	2023A	2024A	2025F	2026F	2027F	2028F
Fixed Assets	6.1	17.1	42.0	56.0	60.3	66.0
Intangible Assets	1.0	1.5	6.4	6.4	6.4	6.4
Other FA	-	-	-	-	-	-
Inventories	-	-	-	-	-	-
Receivables	0.4	17.9	35.2	31.6	41.1	49.3
Other CA	31.5	22.5	7.9	7.9	7.9	7.9
Cash	29.5	24.9	42.5	78.6	438.1	490.2
Total Assets	68.4	83.9	133.9	180.5	553.7	619.8
Payables	7.8	17.3	2.7	7.9	10.3	12.3
ST Borrowings	-	-	-	-	-	-
Other ST Liability	0.6	1.1	1.2	1.2	1.2	1.2
LT Borrowings	2.5	-	-	-	-	-
Other LT Liability	2.5	3.2	2.0	2.0	2.0	2.0
Minorities Int.	-	-	-	-	-	-
Net Assets	45.4	61.1	126.3	173.4	532.3	588.8
Share Capital	2.0	3.0	32.3	44.3	357.0	357.0
Reserves	43.4	58.1	94.1	129.1	175.3	231.8
Equity	45.4	61.1	126.3	173.4	532.3	588.8

Cashflow Statement

FY Mar (RM m)	2023A	2024A	2025F	2026F	2027F	2028F
Operating CF	42.6	4.8	23.7	61.9	61.4	76.7
Investing CF	(33.1)	2.9	(20.6)	(14.0)	(4.2)	(5.7)
Financing CF	(1.5)	(13.6)	15.5	(11.7)	302.3	(18.8)

Financial Data & Ratios

FY Mar	2023A	2024A	2025F	2026F	2027F	2028F
Growth (%)						
Turnover	-	34.8	55.1	32.3	30.0	22.0
EBITDA	-	9.2	35.4	27.1	29.5	25.0
Operating Profit	-	20.3	8.6	33.5	32.3	26.6
PBT	-	21.7	7.0	32.9	32.0	26.5
Core Net Profit	-	17.7	6.6	29.9	32.0	26.5
Profitability (%)						
Gross Margin	59.1	46.8	42.2	42.2	43.2	44.4
EBITDA Margin	51.3	41.6	36.3	34.9	34.7	35.6
Operating Margin	48.9	43.6	30.6	30.8	31.4	32.6
PBT Margin	49.7	44.9	31.0	31.1	31.6	32.7
Core Net Margin	50.1	43.7	30.1	29.5	30.0	31.1
Effective Tax Rate	-0.9	2.5	2.9	5.0	5.0	5.0
ROA	41.9	44.3	33.0	29.7	16.8	13.3
ROE	63.1	63.3	38.3	31.2	17.5	13.9
DuPont Analysis						
Net Margin (%)	50.1	43.7	30.1	29.5	30.0	30.5
Assets Turnover (x)	0.8	1.0	1.1	1.0	0.6	0.4
Leverage Factor (x)	1.3	1.2	0.8	0.7	0.9	0.9
ROE (%)	63.1	63.3	38.3	31.2	17.5	13.9
Leverage						
Debt/Asset (x)	-	-	-	-	-	-
Debt/Equity (x)	-	-	-	-	-	-
Net Cash/(Debt)	29.5	24.9	42.5	78.6	438.1	490.2
Net Debt/Equity (x)	Net cash	Net cash	Net cash	Net cash	Net cash	Net cash
Valuations						
Core EPS (sen)	1.6	1.9	2.0	2.6	3.4	4.3
NDPS (sen)	0.11	0.76	0.69	0.65	0.86	1.09
BVPS (RM)	0.03	0.03	0.07	0.09	0.30	0.34
Core PER (x)	55.2	46.9	44.0	33.8	25.6	20.3
Net Div. Yield (%)	0.1	0.9	0.8	0.7	1.0	1.2
P/BV (x)	34.8	25.9	12.5	9.4	2.9	2.6

Source: Kenanga Research

Peer Table Comparison

Name	Rating	Last Price (RM)	Target Price (RM)	Upside	Market Cap (RM m)	Shariah Compliant	Current FYE	Core EPS (sen)		Core EPS Growth		PER (x) - Core Earnings		PBV (x)	ROE	Net Div. (sen)	Net Div. Yld.
								1-Yr. Fwd.	2-Yr. Fwd.	1-Yr. Fwd.	2-Yr. Fwd.	1-Yr. Fwd.	2-Yr. Fwd.	1-Yr. Fwd.	1-Yr. Fwd.	1-Yr. Fwd.	1-Yr. Fwd.
D&O GREEN TECHNOLOGIES BHD	MP	0.475	0.470	-1.1%	588.8	Y	12/2026	2.1	2.3	132.7%	39.9%	22.4	20.9	0.8	3.8%	1.0	2.1%
FRONTKEN BHD	OP	4.80	5.10	6.3%	8,702.1	Y	12/2026	12.8	13.9	31.9%	8.7%	37.6	34.6	6.7	19.1%	4.0	0.8%
INARI AMERTRON BHD	OP	1.93	2.02	4.7%	7,343.9	Y	06/2026	5.7	7.5	-14.6%	30.6%	33.6	25.7	2.6	7.2%	5.0	2.6%
KELINGTON GROUP BHD	OP	6.96	6.15	-11.6%	6,282.2	Y	12/2026	20.5	21.9	23.4%	6.8%	34.0	31.8	7.8	26.1%	13.0	1.9%
LGMS BHD	OP	0.545	0.580	6.4%	248.5	Y	12/2026	2.9	3.6	30.4%	21.8%	18.7	15.3	1.9	10.5%	2.0	3.7%
MALAYSIAN PACIFIC INDUSTRIES	MP	44.10	38.90	-11.8%	8,793.4	Y	06/2026	104.7	134.1	35.6%	28.0%	42.1	32.9	4.0	9.7%	40.0	0.9%
NATIONGATE HOLDINGS BHD	MP	0.855	0.660	-22.8%	1,934.6	Y	12/2026	4.7	5.7	7.8%	21.1%	18.1	15.0	1.8	10.2%	2.0	2.3%
OPPSTAR BHD	MP	0.785	0.230	-70.7%	503.5	Y	03/2026	(1.6)	1.0	-184.7%	-40.0%	N.A.	79.8	4.0	-8.0%	0.0	0.0%
PIE INDUSTRIAL BHD	MP	1.63	1.28	-21.5%	626.0	Y	12/2026	8.1	8.8	37.6%	8.0%	20.1	18.6	0.9	4.8%	0.0	0.0%
SKP RESOURCES BHD	MP	0.385	0.500	29.9%	601.5	Y	03/2026	5.7	4.4	-24.4%	-22.5%	6.8	8.8	0.5	8.0%	0.0	0.0%
SKYECHIP BHD	OP	0.880	2.00	127.3%	1,580.0	Y	03/2026	2.6	3.4	30.1%	32.1%	33.8	25.6	9.1	31.2%	70.0	79.5%
UNISEM (M) BHD	UP	4.00	2.47	-38.3%	6,452.3	Y	12/2026	5.4	9.5	39.6%	74.6%	73.5	42.1	2.9	4.1%	0.0	0.0%
UWC BHD	OP	5.55	4.70	-15.3%	6,123.5	Y	07/2026	9.0	14.3	143.3%	59.0%	61.9	38.9	10.6	18.7%	0.0	0.0%
PENTAMASTER CORP BHD	MP	4.40	3.95	-10.2%	3,129.8	Y	12/2026	12.1	13.1	39.0%	8.1%	36.3	33.6	3.6	10.4%	2.0	0.5%
INFOMINA BHD	OP	1.19	1.90	59.7%	715.5	Y	05/2026	5.6	7.6	60.7%	34.8%	21.1	15.7	3.6	18.3%	1.0	0.8%
SECTOR AGGREGATE					53,625.5					20.4%	24.3%	37.4	30.1	4.1	11.6%		6.3%

Source: Kenanga Research

ESG

Sustainability-related opportunities

- Energy-efficient compute and AI products: SkyeChip plans to develop compute and AI silicon products to improve system efficiency and reduce power consumption in data centres and AI applications.
- Automotive silicon IP: Expansion into automotive IP, including ISO 26262 functional safety alignment, could open exposure to ADAS and autonomous driving applications.
- 2.5D/3D and chiplet products: CIM silicon dies and I/O chiplets are positioned to reduce data movement, improve performance and improve power consumption for AI and high-performance computing workloads.
- Human capital development: New engineers are required to complete 110 hours of training across 25 modules in their first year, supporting technical capability building.

Sustainability-related risks and disclosure gaps

- Climate disclosure gap: SkyeChip states it has no specific GHG reduction targets, initiatives or reduction plans. GHG emissions are described qualitatively as mainly from electricity consumption, but no Scope 1, Scope 2 or Scope 3 data is disclosed.
- Energy data gap: Energy-saving initiatives include LED lighting, automatic AC scheduling and switching off lights, but there is no quantitative electricity consumption, energy intensity or target disclosed.
- Customer concentration / market risk: China and Taiwan collectively contributed 90.6% of revenue for FPE 31 Oct 2025, indicating geographic concentration risk.

TP adjustment: -3% discount

- **Rationale:** SkyeChip has credible sustainability-linked growth angles through energy-efficient AI, chiplet and automotive silicon IP opportunities. Under the stated framework, a 2.5- Star weighted score implies a -3% TP discount for information and operational risk.

ESG Rating

Criterion	*Rating*
GHG Emissions	★ ★
Energy Management	★ ★
Employee Health & Safety	★ ★ ★
Recruiting & Managing a Global & Skilled Workforce	★ ★ ★
Product Lifecycle Management	★ ★ ★
Intellectual Property Protection & Competitive Behavior	★ ★ ★
Overall	★ ★ ½

☆	denotes half-star
★	-5% discount to TP
★★	-3% discount to TP
★★★	TP unchanged
★★★★	+3% premium to TP
★★★★★	+5% premium to TP

Stock Ratings are defined as follows:

Stock Recommendations

OUTPERFORM	: A particular stock's Expected Total Return is MORE than 10%
MARKET PERFORM	: A particular stock's Expected Total Return is WITHIN the range of -5% to 10%
UNDERPERFORM	: A particular stock's Expected Total Return is LESS than -5%

Sector Recommendations***

OVERWEIGHT	: A particular sector's Expected Total Return is MORE than 10%
NEUTRAL	: A particular sector's Expected Total Return is WITHIN the range of -5% to 10%
UNDERWEIGHT	: A particular sector's Expected Total Return is LESS than -5%

******Sector recommendations are defined based on market capitalisation weighted average expected total return for stocks under our coverage.***

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