Technology

Advanced Packaging - The Next Battleground in Semiconductor Value Chain

NEUTRAL

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SEMICON Southeast Asia 2026 reinforced Malaysia's growing strategic relevance in the global semiconductor value chain, as the country moves beyond traditional assembly and test into higher-value areas such as IC design, advanced packaging, intelligent manufacturing, and supply-chain integration. A key takeaway from the event is that advanced packaging has emerged as a critical enabler of next-generation semiconductor performance, particularly as Moore's Law slows and AI/HPC workloads become increasingly constrained by memory bandwidth, latency, power efficiency and thermal management. No longer merely a back-end assembly process, advanced packaging is now a strategic technology layer that determines how efficiently logic, memory, RF, sensors and power components work together within a system.

For investors, the strongest value creation is likely to be concentrated in AI/HPC-related technologies such as FCBGA, 2.5D/3D integration, HBM, hybrid bonding, high-end substrates and eventually glass substrates, while Malaysia's opportunity remains selective across OSAT, automation, test, precision engineering, photonics packaging and process infrastructure. Malaysia's formation of MAPC (Malaysia Advanced Packaging Consortium) is strategically positive, with a roadmap from pilot validation in 2026 to C4 bumping in 2027 and 2.5D packaging capability by 2028. Key names to watch under this theme include MAPC members, namely SkyeChip (OP: RM2.00), Inari (OP, TP: RM2.42), FusionAP S/B, Pentamaster (MP, TP: RM3.95) and NSW Automation S/B.

Overall, we maintain our NEUTRAL call for the sector and continue to favour KGB (OP, TP: RM9.05), UWC (OP, TP: 4.70), FRONTKN (OP, TP: RM5.10) and INFOMINA (OP, TP: RM1.90) as our top pick for the sector due to their stronger order visibility, margin resilience and AI/front-end exposure, while staying cautious on EMS names given weak end-demand and FX sensitivity.

We recently attended SEMICON Southeast Asia 2026, held from 5–7 May 2026 at the Malaysia International Trade and Exhibition Centre (MITEC). The event reinforced Southeast Asia's rising strategic importance in the global semiconductor value chain, with Malaysia increasingly positioning itself beyond traditional assembly, test and packaging into higher-value areas such as IC design, advanced packaging, intelligent manufacturing and supply-chain integration. Themed "Transform Tomorrow", the event attracted close to 21,000 attendees from over 65 countries/regions, with more than 700 exhibitors across 1,519 booths. Key highlights centered on AI and intelligent manufacturing, advanced packaging and heterogeneous integration, sustainability, supplier sourcing and SME capability building, in line with Malaysia's National Semiconductor Strategy. Overall, the event underscored Malaysia's growing relevance as a regional semiconductor hub, particularly as global supply chains diversify and demand for AI/HPC, advanced manufacturing and packaging capabilities continues to accelerate.

Exhibit 1: SEMI South East Asia 2026

Source: SEMI, Kenanga Research

Exhibit 2: SEMI South East Asia 2026

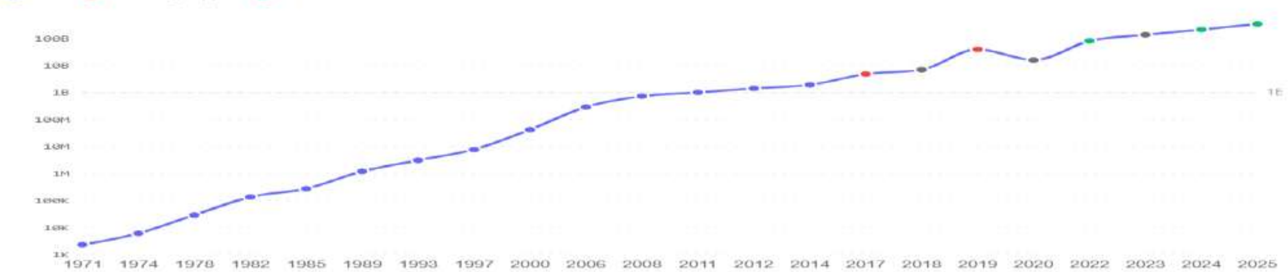
Source: SEMI, Kenanga Research

Moore’s Law is slowing; advanced packaging takes centre stage.
Advanced packaging has emerged as a critical pathway to extend semiconductor performance scaling as traditional Moore’s Law becomes increasingly constrained. While chip performance has historically been driven by transistor shrinking and migration to more advanced process nodes, this approach is becoming more challenging due to EUV limitations, rising process complexity, higher design costs and weaker economics at leading-edge nodes. As a result, the industry is shifting from pure transistor-level scaling towards system-level (or integrated circuit) scaling. To recap, Moore’s law is the observation that the number of transistors in an integrated circuit doubles about every two years, thanks to improvements in production. While this trend held remarkably well for several decades, Intel’s former CEO Pat Gelsinger acknowledged in 2023 that the industry is no longer in the “golden era” of Moore’s Law, with effective transistor doubling now closer to every three years, reflecting the growing technical and economic challenges of further scaling. (see exhibit 3 and 6)

Rather than relying on one large monolithic chip, chipmakers are increasingly integrating multiple specialised dies within a single package through chiplets, heterogeneous integration, fan-out packaging, 2.5D/3D integration, hybrid bonding and emerging glass substrates. By bringing logic, memory, RF, sensors and power components closer together, advanced packaging helps improve bandwidth, reduce latency, lower power consumption and enhance overall system performance.

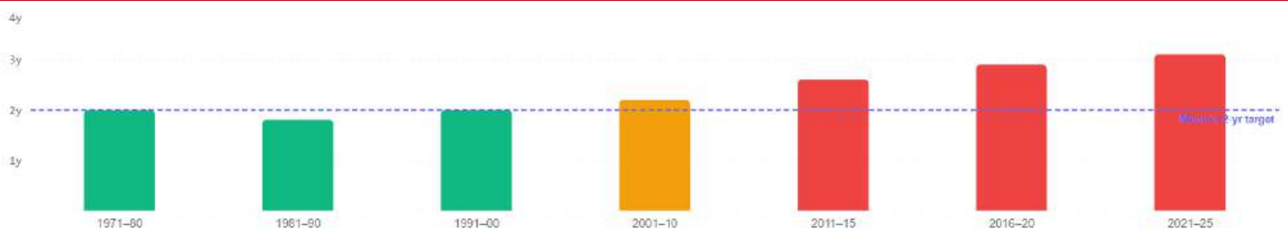
In short, advanced packaging is no longer merely a back-end assembly process. It is becoming a strategic technology layer that determines how efficiently multiple chips work together within a single system. This is particularly important for AI/HPC, automotive, mobile and networking applications, where performance increasingly depends not only on the capability of each chip, but also on how quickly and efficiently data can move between logic and memory.

Exhibit 3: Moore’s Law – Transistor Count (1971-2025)



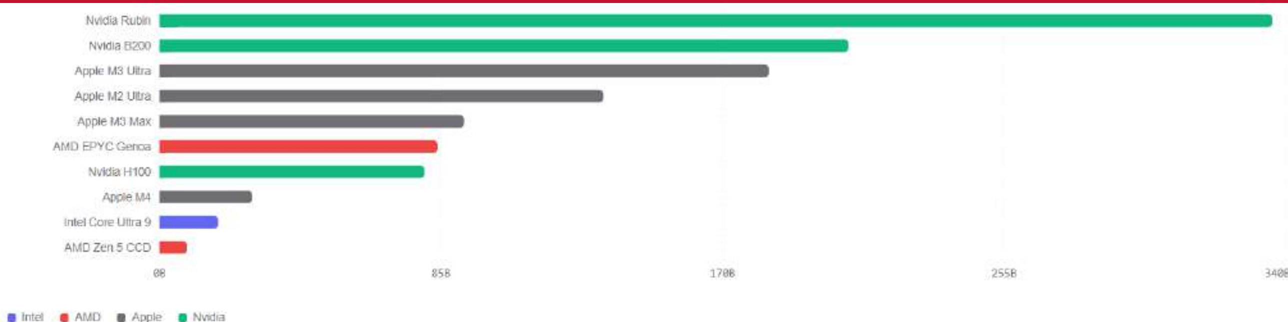
Source: Value Add VC Kenanga Research

Exhibit 4: Moore’s Law is Slowing Down



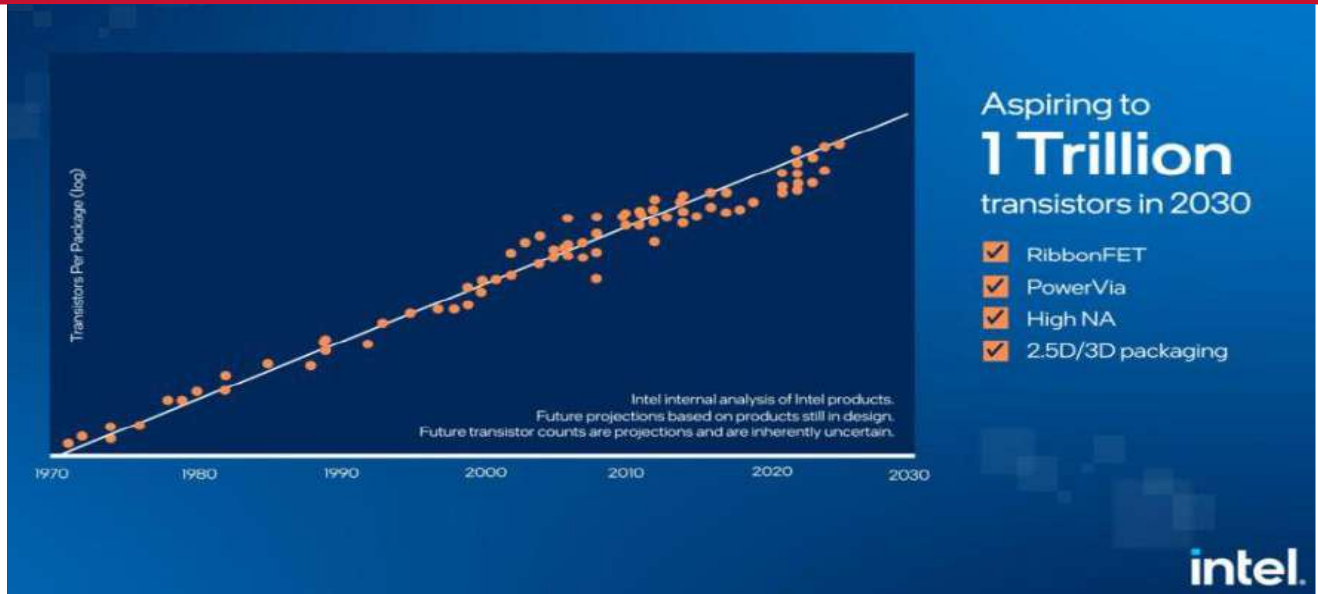
Source: Value Add VC, Kenanga Research

Exhibit 5: Moore’s Law – Who Packs the Most Transistors?



Source: Value Add VC, Kenanga Research

Exhibit 6: Moore's Law – Intel aspiring to 1T transistors in 2030

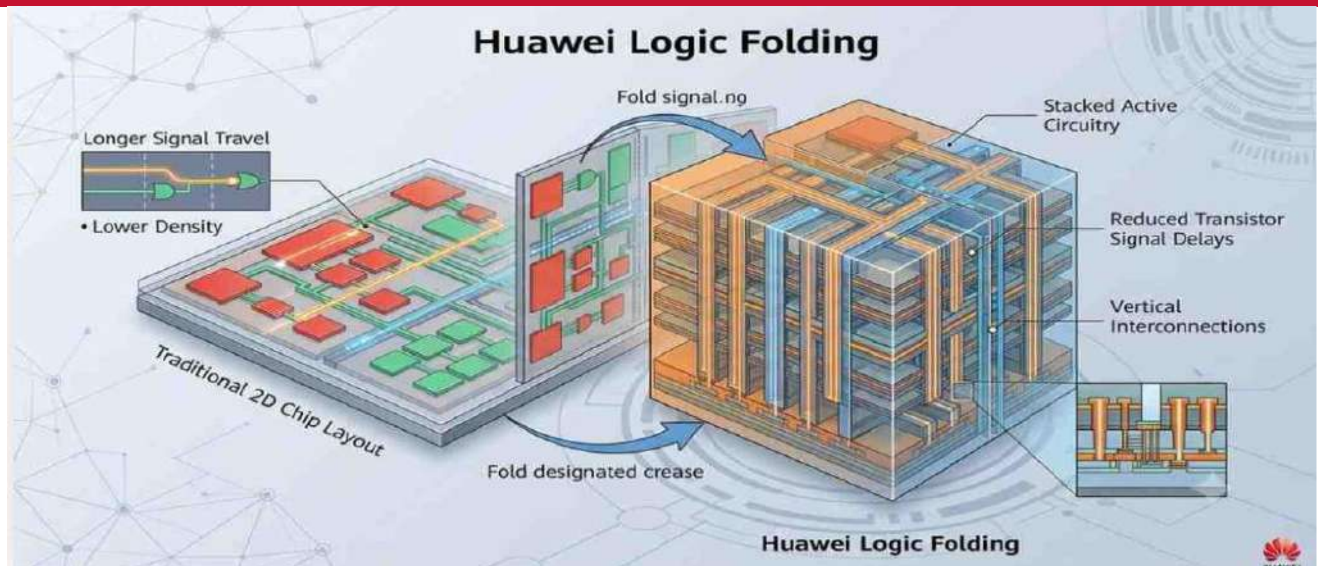


Source: Intel, Kenanga Research

Tau Law is Huawei's proposed post-Moore framework that shifts the focus from shrinking transistors to reducing data transmission delay across chips, packages and systems. While *Moore's Law improves performance mainly by fitting more transistors into a smaller area, Tau Law aims to improve performance by shortening signal paths, enhancing interconnect efficiency and optimising chip/system architecture*. In layman terms, Moore's Law is about making the chip "smaller and denser", while Tau Law is about making data "travel faster and more efficiently".

The opportunity lies in advanced packaging, chiplets, HBM integration, optical interconnects and system-level optimisation, especially as AI/HPC workloads become increasingly constrained by memory bandwidth and data movement. However, execution remains challenging due to Huawei's limited access to leading-edge lithography, EDA tools, advanced equipment and global supply chains. Huawei presented Tau Scaling Law at IEEE ISCAS 2026, claiming 381 chips had been designed and mass-produced using this principle, while its upcoming Kirin chips are expected to adopt the Logic Folding architecture. According to Huawei, its Logic Folding architecture can improve efficiency, reduce delays, and increase transistor density without requiring a major reduction in transistor size. The concept focuses on improving chip architecture rather than simply making transistors smaller.

Exhibit 7: Huawei Logic Folding Architecture



Source: Huawei, Kenanga Research

Why advanced packaging matters now?
Advanced packaging is becoming increasingly important because traditional chip packaging is no longer enough to meet the performance, power efficiency and miniaturisation requirements of modern electronics.The main purpose of advanced packaging is to place chips closer together, improve data transfer speed, reduce power consumption and allow more functions to be integrated into smaller devices.

Modern applications such as AI data centres, autonomous driving, 5G/6G networks, smartphones and high-performance computing require chips to process more data at higher speeds, while consuming less power and occupying less space. Traditional chip scaling remains important, but it is no longer sufficient on its own to meet these rising requirements. This is why the industry is increasingly using packaging innovation to integrate multiple chips more closely within the same package. The strongest driver is AI. In AI computing, performance is not determined solely by processor speed, but also by how quickly data can move between the processor and memory. This explains the growing importance of high-bandwidth memory and 2.5D/3D packaging. By placing logic and memory closer together, advanced packaging shortens data travel distance, improves bandwidth and latency, and enhances energy efficiency. For investors, this means advanced packaging is directly tied to the AI infrastructure build-out, rather than being just a traditional assembly and test theme.

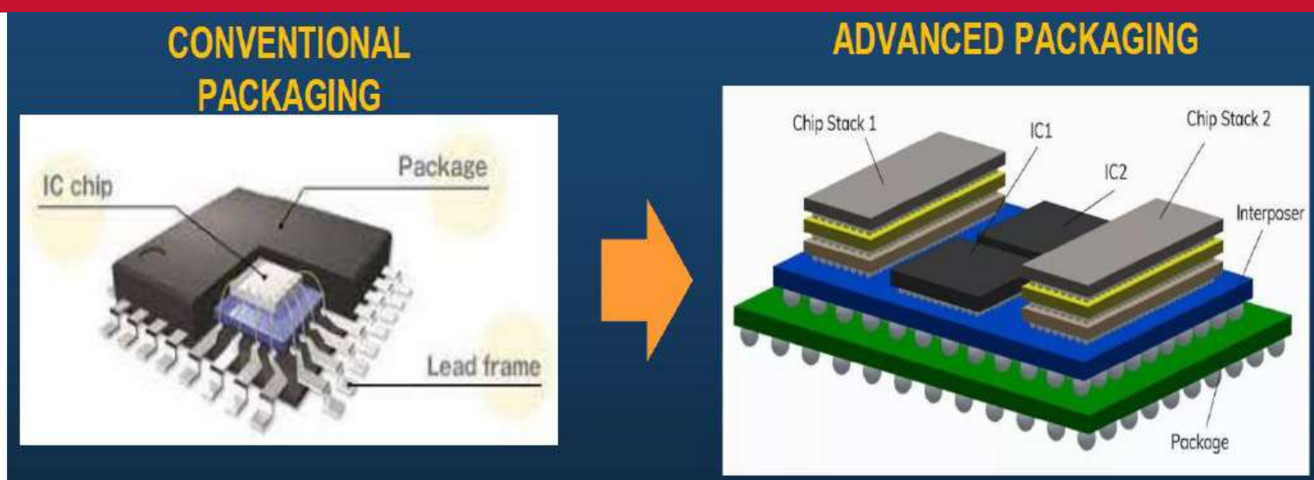
Another key driver is the shift towards chiplet architecture. Instead of building one large chip that contains all functions, chipmakers are increasingly splitting designs into smaller functional blocks, or "chiplets", and integrating them within a single package. This allows each function to be manufactured using the most suitable process technology — for example, advanced logic on leading-edge nodes, while I/O, analogue, RF or memory components can remain on mature nodes. In this model, the package becomes the platform that connects all chiplets together, making advanced packaging increasingly central to future semiconductor performance and value creation.

What is advanced packaging – in simple terms.
At its core, advanced packaging refers to a group of technologies used to connect and integrate chips more efficiently after the wafer fabrication stage. *Traditional packaging mainly protects the chip and connects it to the circuit board. Advanced packaging goes further by improving the way different chips and components communicate with each other.* It is not just about enclosing the chip, but about improving system-level performance.

A simple way to explain this is to compare a semiconductor device to a city. The individual chips are like buildings, while the packaging technology is like the road, railway and communication network that connects them. If the roads are slow or congested, the city cannot function efficiently, even if the buildings are very advanced. Similarly, in modern semiconductors, a powerful processor is not enough if data cannot move quickly between logic, memory and other components. Advanced packaging improves this "connectivity network" inside the chip package. In other words, advanced packaging is no longer just about "wrapping" the chip. It is now about designing how multiple chips communicate, share power, manage heat and work together as one high-performance system.

This is why advanced packaging is becoming more important in AI, mobile, automotive and networking applications. These end-markets require more functions to be packed into smaller spaces, while also demanding better performance and lower power consumption. Advanced packaging enables this by supporting higher interconnect density, shorter signal paths, better thermal management and more compact system integration.

Exhibit 8 Conventional vs. Advanced Packaging



Source: MAPC, Kenanga Research

Advanced packaging technologies segmentation: Not all are the same

One of the most important points for investors to understand is that advanced packaging is not a single technology. It covers a wide spectrum of solutions, each with different cost, performance and end-market characteristics. Some technologies are mature and volume-driven, while others are high-growth and closely tied to AI/HPC. A general description of these technologies are in the 8 points below, whereas the technical diagram and description, challenges it overcomes, and the global and local players in the supply chain are detailed in exhibit 10 and 11. Broadly, companies that are exposed to advanced packaging in Malaysia include Inari, MPI, and Unisem, and we our preferred proxy is via Inari.

(i) ***Fan-in/wafer-level chip-scale packaging*** is typically used for small, compact and cost-sensitive chips. It is widely used in smartphones, consumer electronics, power management ICs, audio chips, WiFi modules, and image sensors. Its advantage is that it keeps the package size close to the die size, making it suitable for high-volume compact devices. However, it is more mature compared with newer technologies such as 2.5D/3D packaging.

(ii) ***Fan-out packaging*** extends the connection area beyond the original chip footprint by using redistribution layers. In simple terms, it gives the chip more room to connect to the outside world without relying heavily on a traditional substrate. This makes fan-out useful for mobile, RF, radar, power management and selected processor applications. It could also gain more strategic relevance if high-end substrate capacity becomes tight, as fan-out can reduce reliance on conventional substrates in certain designs.

(iii) ***FCCSP (Flip-Chip Chip-Scale Package) and FCBGA (Flip-Chip Ball Grid Array)*** are both flip-chip-based packages, but they serve different performance requirements. FCCSP is generally used for smaller, compact devices such as RF chips, radar, mobile processors and memory-related applications. FCBGA, on the other hand, is used for larger, higher-performance chips such as CPUs, GPUs, AI ASICs and FPGAs. For investors, FCBGA has the clearest AI/HPC read-through because it is widely used in high-performance processors and data-centre applications.

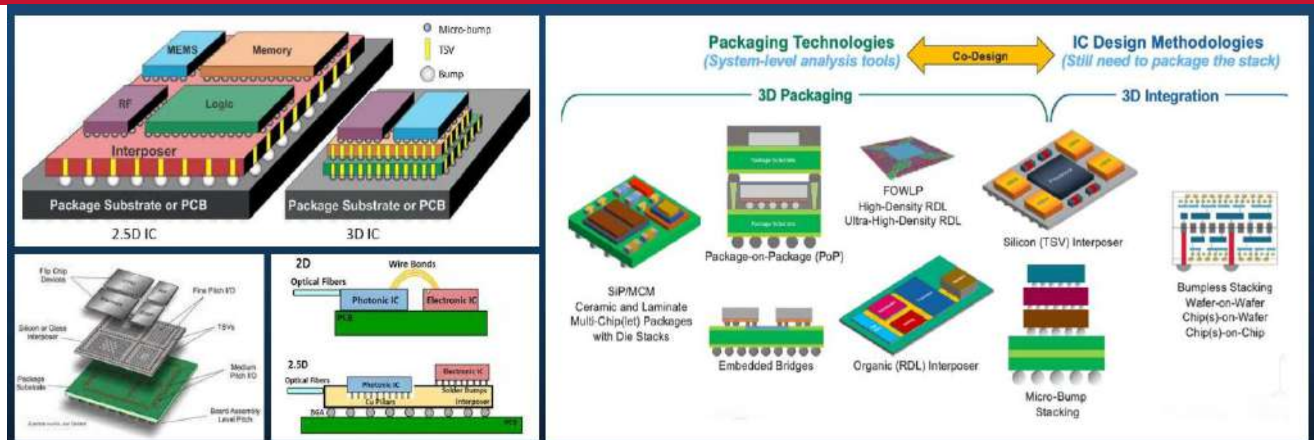
(iv) ***2.5D packaging*** is one of the most important technologies in the AI era. It places multiple chips side-by-side on an interposer, which acts as a high-speed bridge between logic and memory. This is commonly used to connect GPUs or AI accelerators with high-bandwidth memory. ***3D stacking*** goes one step further by stacking chips vertically, reducing the distance between chips and improving bandwidth and power efficiency. These technologies are increasingly critical for AI accelerators, HBM, networking switches and high-performance computing.

(v) ***System-in-Package (SiP)***, integrates multiple dies and components into a compact module. It is commonly used in RF modules, MEMS sensors, audio devices, memory, touch controllers and connected devices. SiP is more about miniaturisation and functional integration, rather than pure computing performance. It remains important for mobile, wearables, IoT and automotive electronics, where space saving and multi-function integration are key requirements.

(vi) ***Hybrid bonding*** is an emerging high-end technology that enables very fine-pitch direct die-to-die bonding. Compared with conventional micro-bump connections, hybrid bonding allows chips to be connected more densely and efficiently. This is important for future 3D integration, advanced memory, image sensors and potentially next-generation AI processors.

(vii) ***Glass substrates*** are next-generation packaging materials that enable finer routing, lower signal loss and better power efficiency versus conventional organic substrates. They are promising for AI/HPC chip packages, but manufacturing remains challenging due to the need to create tiny through-glass vias without cracking the glass.

Exhibit 9: Advanced Methods of Packaging Chips



Source: MAPC, Kenanga Research

Exhibit 10: Advanced Packaging Technologies - 1

Technology	Diagram	Description	Bottleneck / Problem Addressed	Maturity	Key Global Players	Key Malaysia Players
Fan-In / Wafer-Level Chip Scale Packaging (WLCSP / FI-WLP)	Fan-In / WLCSP Silicon Die PCB Board	I/O redistribution is confined within the die footprint; solder balls are placed directly on the active surface, making the package identical in size to the die.	Challenge: I/O density and signal integrity for high-speed interfaces. Technical fix: Flip-chip interconnects shorten signal paths, reduce inductance, and support PCIe, DDR, and HBM interfaces — the standard package for CPUs, GPUs, and ASICs. Layman term: Instead of wiring the chip from the top, you flip it upside down and plug it in directly via tiny solder bumps — like a USB drive inserted face-down. Shorter path = faster signal, less heat.	Mature (mainstream)	TSMC, ASE Group, Amkor, JCET, Tongfu Microelectronics	Unisem offers Wafer Level CSP, wafer bumping, probing and full wafer-map integration. MPI and Inari have broader OSAT/flip-chip-related capabilities
Fan-Out Wafer/Panel-Level Packaging (FOWLP / FOPLP)	Fan-Out (FOWLP) Silicon Die PCB Board	Die(s) embedded in a reconstituted moulded wafer/panel; RDL (redistribution layer) layers extend routing beyond the die edge, enabling higher I/O density without a traditional substrate. Key variants: TSMC InFO, ASE FOCoS, Amkor SWIFT.	Challenge: Interconnect density vs. substrate cost trade-off. Technical fix: Removes costly organic substrate for mid-tier products; shorter signal paths improve speed and thermal performance — critical for mobile AP + PMIC co-integration. Layman term: The chip needs more connection points than its size allows. Fan-out 'extends' the chip onto a moulded platform — more exits, no expensive circuit board underneath.	Mature–Advanced (HVM for mobile; panel-level emerging)	TSMC (InFO), Samsung (FO-PLP), ASE (FOCoS), Amkor (SWIFT), JCET, PTI	Unisem has wafer-level packaging and wafer bumping capability. Inari has the fan-out/CPO adjacency through optoelectronics and advanced SiP

Source: Various sources, Kenanga Research

Exhibit 11: Advanced Packaging Technologies - 2

Technology	Diagram	Description	Bottleneck / Problem Addressed	Maturity	Key Global Players	Key Malaysia Players
System-in-Package (SiP)		Multiple heterogeneous dies, passives, and MEMS/sensors integrated into a single package module — replicating entire PCB functionality. Can use wire bond, flip-chip, or embedded die techniques.	Challenge: System miniaturisation and multi-function integration. Technical fix: Combines RF, baseband, power, and memory into one compact module — the enabling technology for wearables, hearables, IoT, and automotive radar. Apple Watch is the canonical example. Layman term: Instead of building a circuit board and populating it with separate chips, SiP bundles everything into one fingernail-sized module. The whole 'board' becomes a single package.	Mature–Advanced (mainstream for wearables; complex SiP at leading edge)	ASE Group (Apple Watch SiP leader), Amkor, JCET, Murata, TDK (RF SiP)	Inari offers advanced SiP assembly and test, fine-pitch SMT, high-speed/high-accuracy flip-chip die placement, moulded underfill and final testing capability. Unisem also offers MCM/SIP and stacked-die package options, while MPI/Carsem has module and sensor packaging exposure.
Flip-Chip CSP / BGA (FCCSP / FCBGA)		Die connected face-down to an organic substrate via C4 solder bumps or copper pillars (CuPillar). FCCSP targets mobile; FCBGA addresses high-performance compute with large substrates.	Challenge: I/O density and signal integrity for high-speed interfaces. Technical fix: Flip-chip interconnects shorten signal paths, reduce inductance, and support PCIe, DDR, and HBM interfaces — the standard package for CPUs, GPUs, and ASICs. Layman term: Instead of wiring the chip from the top, you flip it upside down and plug it in directly via tiny solder bumps — like a USB drive inserted face-down. Shorter path = faster signal, less heat.	Advanced-Mainstream (FCCSP); Advanced-Mainstream (FCBGA)	Amkor, ASE Group, JCET, PTI; Ibiden / Shinko / AT&S (substrates)	Inari (flip-chip & advanced SiP capability); MPI (substrate based packaging, power packages, SiC/GaN, automotive & AI server related packaging)

Source: Various sources, Kenanga Research

Exhibit 12: Advanced Packaging Technologies - 3

Technology	Diagram	Description	Bottleneck / Problem Addressed	Maturity	Key Global Players	Key Malaysia Players
2.5D Packaging (Silicon Interposer / Bridge)	2.5D Packaging (CoWoS / Interposer)	Multiple dies (logic + HBM) mounted side-by-side on a silicon interposer or organic/glass bridge. Ultra-fine RDL wiring connects dies at <55 µm pitch. Platforms: TSMC CoWoS-S/L/R, Intel EMIB, Samsung I-Cube.	Challenge: Memory bandwidth wall for AI/HPC accelerators. Technical fix: HBM requires thousands of micro-bumps at pitches unachievable on PCB — only a silicon interposer delivers the bandwidth density needed for GPU + HBM co-packaging (NVIDIA H/B series, AMD MI series). Layman term: The GPU is the engine; HBM memory is the fuel tank — and they need an extremely wide pipe between them. The silicon interposer is that pipe, enabling data to flow at speeds no standard circuit board can match.	Advanced (HVM for AI/HPC; capacity-constrained)	TSMC (CoWoS — dominant), Samsung (I-Cube), Intel (EMIB), ASE (CoWoS-R OSP), Amkor	No direct Malaysian HVM player currently; Inari/MPI/Unisem as adjacent only
3D Packaging (3D-IC / Die Stacking via TSV)	3D Packaging (TSV Die Stacking)	Dies stacked vertically and interconnected via Through-Silicon Vias (TSVs) or hybrid bonding — eliminating lateral routing. Examples: HBM (DRAM via TSV), AMD 3D V-Cache (TSMC SoIC), Intel Foveros.	Challenge: Compute-memory latency and bandwidth density. Technical fix: TSV vertical interconnects deliver 10–100× bandwidth improvement over 2D routing — critical for cache-sensitive workloads and CIS stacking. Layman term: Rather than placing chips side-by-side on a flat board like houses on a street, 3D stacking builds them like floors of a skyscraper — connected by vertical 'elevator shafts' (TSVs). Data travels a fraction of the distance.	Advanced–Emerging (TSV/HBM in HVM; logic-on-logic at leading edge)	SK Hynix / Samsung / Micron (HBM via TSV), TSMC (SoIC), Intel (Foveros), ASE, Amkor	Unisem and Inari as limited/adjacent; not direct HBM stack players

Source: Various sources, Kenanga Research

Exhibit 13: Advanced Packaging Technologies - 4

Technology	Diagram	Description	Bottleneck / Problem Addressed	Maturity	Key Global Players	Key Malaysia Players
Hybrid Bonding (Direct Bond Interconnect / DBI)		Die-to-die or die-to-wafer bonding via direct Cu-to-Cu and oxide-to-oxide fusion — no solder bumps. Achieves sub-micron (<1 μm) bond pitch. Platforms: TSMC SoIC-X, Sony/Samsung CIS stacking, Xperi DBI.	Challenge: Micro-bump pitch limits and interconnect power loss. Technical fix: Removes solder bumps entirely, enabling orders-of-magnitude higher I/O density, near-zero signal loss, and lower power between stacked dies — essential for logic-on-logic and next-gen CIS. Layman term: Traditional chip stacking uses tiny solder bumps — but these bumps are getting too large as chips get denser. Hybrid bonding eliminates them entirely, fusing copper pads directly like welding metal surfaces at atomic scale.	Emerging–Early Adoption (CIS in HVM; logic-on-logic at TSMC/Intel)	TSMC (SoIC-X), Sony Semiconductor (CIS), Samsung, Intel, EV Group / SUSS (bonding equipment), Adeia/Xperi (IP)	Pentamaster (precision alignment handlers relevant to bonding workflows); No direct HVM exposure among Malaysian OSATs currently
Glass Substrates (Through-Glass Via / TGV)		Organic laminate (BT/ABF) replaced with glass panels as the interposer or package core. Glass offers superior dimensional stability, ultra-low CTE, higher via density (TGV), and finer RDL surface. Intel leads commercialisation (2026+ target).	Challenge: Substrate warpage and scalability limits for next-gen chiplet packages. Technical fix: Organic substrates bow and warp at large panel sizes — limiting chiplet scaling beyond current reticle limits. Glass resolves the substrate bottleneck for AI accelerators requiring larger FCBGA/2.5D form factors. Layman term: Today's chip packages sit on a fibreglass board that warps under heat, like a biscuit going soft. Glass is flatter, more stable, and supports far finer wiring — upgrading from a dirt road to a precision-engineered data highway.	Pre-Commercial / Early Development (2026–2028 ramp expected)	Intel (pioneer, 2026 target), Corning / AGC / NEG (glass supply), DNP / Ibiden (glass core R&D), Applied Materials (TGV etch)	No direct HVM exposure among Malaysian-listed companies currently; potential longer-term adjacency in substrate test and inspection

Source: Various sources, Kenanga Research

End market mapping – matching technologies with applications

For investors, mapping advanced packaging technologies to their end-market exposure helps identify where growth and value are concentrated. AI/HPC is currently the highest-growth and highest-value segment, driven by strong demand for FCBGA, 2.5D interposers, 3D stacking, HBM integration, hybrid bonding and high-end substrates. These technologies are critical as AI accelerators require ultra-fast processor-to-memory communication, high interconnect density and robust thermal management.

Mobile and consumer electronics remain key volume markets, although growth is more mature. These applications typically rely on fan-in, fan-out, FCCSP and SiP, where the main requirements are compact form factor, low power consumption, cost efficiency and multi-function integration. Key use cases include smartphones, wearables, RF modules, audio chips, camera sensors and connectivity modules.

Automotive is an increasingly important structural growth market, supported by rising semiconductor content in EVs, Advanced Driver Assistance Systems (ADAS) and connected vehicles. Packaging demand is driven by radar, sensors, power devices, connectivity modules, domain controllers and automotive processors. However, the segment carries longer qualification cycles and stricter reliability standards, requiring suppliers to demonstrate strong quality consistency, thermal stability and long product lifecycle support.

Networking and optical applications are also gaining relevance, particularly as AI data centres scale and data movement becomes a system-level bottleneck. This supports demand for silicon photonics, optical engines and, longer term, co-packaged optics, where optical components are placed closer to switching chips to improve bandwidth and power efficiency. While still emerging, this segment could become increasingly important as AI clusters become larger and more power-intensive.

According to advanced packaging report by Yole Group, an international semiconductor-focused market research and strategy consulting firm, the table below maps the key packaging technologies to their respective end-market applications.

Exhibit 14: Advanced Packaging - End-market Applications

ADVANCED PACKAGING					
WLCSP / Fan-In Packaging	**Fan-Out Packaging**	**FCBGA Packaging**	**FCCSP Packaging**	**System-in-Package (SiP)**	**2.5D / 3D-Stacked Packaging**
APPLICATIONS					
PMIC / Power IC	PMIC / Power IC	CPU	Memory / DDR / DRAM	RF Connectivity	xPU for HPC
Audio Codec	Audio Codec	GPU	RF IC / Radar	MEMS & Sensors	AI Accelerator
WiFi Module	RF Switch / Radar	APU	APU	Memory	Networking Switch
Display IC / Driver IC	APU / other xPU	AI ASIC	-	Touch Controller	Mobile Processor
CIS		FPGA	-	Audio SiP	Memory
PRIMARY END-MARKETS					
Mobile & Consumer (100%)	Mobile & Consumer (91%)	Mobile & Consumer (56%)	Infrastructure (52%)	Mobile & Consumer (90%)	Infrastructure (60%)
	Infrastructure (6%)	Automotive (22%)	Mobile & Consumer (47%)	Industrial (6%)	Mobile & Consumer (37%)
	Automotive (3%)	Infrastructure (21%)	Automotive (1%)	Automotive (3%)	Industrial (3%)
				Infrastructure (1%)	
EMERGING APPLICATIONS					
IoT Sensors	AI Edge Device	AI Accelerators	Mobile Processor	Wearables / Hearables	AI / ML Accelerators
Wearables	Wearable Electronics	HPC / Data Centre	WiFi	Smart Home Devices	Networking / CPO
Low-cost Consumer Devices	Optical Engine		Automotive MCU	Medical IoT	Edge Computing
KEY CHARACTERISTICS					
Wafer-level CSP; compact, low-cost	Redistribution Layer (RDL) fan-out beyond die edge	Flip-chip on organic substrate; high-speed I/O	Fine-pitch flip-chip on CSP substrate	Heterogeneous integration of multiple components in single package	Interposer (2.5D) or die-on-die (3D) with TSV/μbumps
Ultra-thin, smallest form factor	Thin, low-profile; medium I/O density	Large format; high I/O density	Mid-size; mid-to-high I/O density	Module format; highest integration	High-density; large die area
TECHNOLOGY MATURITY					
Very High – commodity	High – mainstream	High – mainstream	High – mainstream	High – established for consumer	Medium-High – rapidly scaling
Cost pressure driving to FCBGA for complex ICs	Expanding into AI edge & automotive	Dominant for AI ASICs & HPC CPUs	Transitioning some designs to FCBGA	Expanding into medical & industrial IoT	Core technology for HBM & AI chips

Source: Yole Group, Kenanga Research

Market size and growth outlook

The market outlook for advanced packaging is attractive. According to Yole's study, the advanced packaging market is expected to grow from around USD54b in 2025 to USD109b by 2031, implying a 14% CAGR. This growth is underpinned by rising semiconductor content across AI, HPC, automotive, mobile, networking and consumer electronics. Importantly, growth is not only volume-driven, but also value-driven, as packages become more complex and command higher value per unit.

Within the market, 2.5D/3D stacked packaging appears to be the most structurally attractive segment, with Yole indicating a CAGR of around 21%. This is mainly driven by AI/HPC and HBM integration. As AI models become larger and more data-intensive, processors need faster access to memory. This increases the need for 2.5D interposers, high-end substrates, fine-pitch interconnects and advanced bonding technologies.

The implication for investors is that advanced packaging growth will be uneven across segments. Mature technologies such as WLCSP and some SiP applications will continue to benefit from mobile and consumer volumes, but the strongest value creation is likely to come from AI/HPC-related packaging. This is where performance requirements are highest, package complexity is greatest, and pricing power is likely to be stronger.

Technology roadmap – where the industry is heading

The advanced packaging roadmap is moving towards higher I/O density, finer pitch, better integration and larger package sizes. In simple terms, future chips need more connection points, shorter communication paths and better thermal control. This is driving the industry from conventional wire bond and fan-in packages towards fan-out, flip-chip, FCBGA, 2.5D interposers, 3D stacking, hybrid bonding and glass-core substrates.

One major trend is the shift from monolithic SoC design to chiplet-based heterogeneous integration. Instead of using one large die, chipmakers can combine multiple smaller dies in one package. This allows better design flexibility, improves yield and enables different functional blocks to use different process nodes. For example, a high-performance AI chip may combine logic, HBM, I/O and accelerators in one package. This makes packaging a critical part of chip architecture.

Another key trend is the transition from micro-bump stacking to hybrid bonding. Micro-bumps are currently widely used to connect stacked chips, but as interconnect pitch becomes smaller and bandwidth requirements increase, hybrid bonding offers a more advanced solution. It enables more direct and denser chip-to-chip connections, which can improve speed and power efficiency. This technology is still developing, but it is likely to become increasingly important for next-generation 3D integration.

Panel-level packaging is also gaining attention as the industry seeks to reduce cost and improve manufacturing efficiency. Compared with wafer-level packaging, panel-level packaging uses larger rectangular panels, potentially allowing more units to be processed at the same time. This could lower cost over time, although technical challenges such as warpage, yield control and process uniformity remain important.

Co-packaged optics (CPO) is another longer-term trend. As AI data centres become larger, electrical interconnects may struggle to keep up with bandwidth and power-efficiency requirements. Optical interconnects can help address this by improving data transmission efficiency. Co-packaged optics brings optical engines closer to the processor or switch chip, reducing power loss and improving data movement. While adoption may take time, it represents an important future direction for AI networking.

Bottlenecks and value pools

As advanced packaging becomes more complex, several bottlenecks are emerging across the supply chain. The first is high-end substrate capacity. AI processors and HBM-based packages require large, complex and high-quality substrates. If AI demand continues to absorb more substrate capacity, this could create tightness and support alternative packaging approaches such as fan-out, RDL interposers, mold interposers and glass-core substrates.

Interposers are another key bottleneck. In 2.5D packaging, the interposer acts as the bridge between logic and memory. It must support very high-density connections and strong signal integrity. Silicon interposers are widely used in high-end AI/HPC packages, but alternative solutions such as RDL interposers and mold interposers are being developed to address cost and scalability requirements.

Precision die placement is also becoming more critical. In fan-out and chiplet-based packaging, dies must be placed accurately before redistribution layers or interconnects are formed. Any die shift or misalignment can affect yield and performance. This increases the importance of advanced placement equipment, inspection tools, adaptive patterning and process control.

Thermal management is another major issue. AI processors consume significant power and generate substantial heat. As more dies are packed closer together, managing heat becomes more difficult. This creates opportunities for advanced thermal interface materials, package design, substrates, underfill, molding materials and cooling-related solutions.

Inspection and test will also become increasingly important. As packages integrate more chips and interconnects, the cost of failure rises. A defect in one component or interconnect can affect the entire package. This increases the need for advanced inspection, electrical test, optical test, reliability screening and yield-management solutions. In our view, test and inspection are likely to become more valuable parts of the advanced packaging ecosystem.

Who benefits globally

Globally, the key beneficiaries of advanced packaging are likely to be foundries, OSATs, substrate suppliers, equipment vendors, materials suppliers and EDA/design ecosystem players. Among foundries, TSMC, Samsung Electronics and Intel are well positioned, given their growing emphasis on integrating front-end wafer technology with advanced back-end packaging platforms. This is increasingly important for AI/HPC customers, where chip performance depends not only on leading-edge process nodes, but also on how efficiently logic, memory and other chiplets are integrated within the package. In this context, advanced packaging has become a strategic battleground for leading foundries, particularly in 2.5D/3D integration, chiplet packaging, hybrid bonding and high-bandwidth memory integration.

OSATs should also benefit, especially those with capabilities beyond conventional assembly and test. Leading global OSAT players such as ASE Technology and Amkor Technology are better positioned to capture demand from fan-out, SiP, flip-chip, 2.5D/3D packaging and advanced test solutions. As customers increasingly require higher-density interconnects, finer-pitch assembly, better thermal control and more complex package-level testing, larger OSATs with stronger technical capabilities, scale and customer qualification should gain share. However, the gap between leading OSATs and smaller players may widen, as advanced packaging requires higher capex, stronger process know-how and deeper engineering collaboration with customers.

Substrate suppliers are another important beneficiary group. High-end FCBGA and AI substrates are becoming increasingly critical for GPUs, CPUs, AI ASICs, FPGAs and networking chips. Key global substrate players include Ibiden, Shinko Electric, and Unimicron. As AI packages become larger and more complex, substrate requirements are also rising in terms of layer count, routing density, signal integrity, thermal performance and warpage control. This should support longer-term demand for high-end substrate capacity, while also accelerating industry interest in next-generation platforms such as glass-core substrates.

Equipment suppliers should benefit from the rising process complexity in advanced packaging. Companies such as Applied Materials, Lam Research, KLA, and Tokyo Electron are exposed to different parts of the advanced packaging value chain, including deposition, plating, lithography, bonding, die attach, wafer thinning, dicing, inspection and test. As packaging moves towards finer pitches, hybrid bonding, 2.5D/3D integration and panel-level processes, the need for more precise equipment and stronger process control should increase. This makes equipment vendors one of the clearer beneficiaries of the advanced packaging capex cycle.

Materials suppliers should also see rising opportunities as packages become more complex and performance requirements become more demanding. Key beneficiaries may include companies such as Ajinomoto, Resonac, JSR, Shin-Etsu Chemical, Sumitomo Chemical, DuPont, Henkel and Namics, which supply materials such as build-up films, underfill, mold compounds, photoresists, dielectric materials, adhesives and other advanced packaging consumables. As package complexity increases, material performance becomes more critical in areas such as thermal management, warpage control, reliability and signal integrity.

Finally, EDA and design ecosystem players such as Synopsys, Cadence and Siemens EDA should also benefit from the shift towards chiplets and heterogeneous integration. Advanced packaging increasingly requires chip-package-system co-design, where the chip, package and board must be designed together to optimise performance, power and cost. As more companies adopt chiplet-based architectures, design tools for simulation, interconnect planning, thermal modelling, signal integrity and package verification should become increasingly important.

Overall, the advanced packaging opportunity is broad, but the strongest beneficiaries are likely to be companies with exposure to AI/HPC-related packaging, high-end substrates, 2.5D/3D integration, hybrid bonding, advanced test, precision equipment and enabling materials. In our view, the value pool is shifting towards players that can solve the industry’s most difficult packaging challenges — namely bandwidth, latency, power efficiency, thermal control and yield management.

Malaysia investment read-through

For Malaysia, the advanced packaging read-through is positive but selective. The country’s established OSAT and semiconductor support ecosystem provides a strong base, but the bigger opportunity lies in moving beyond conventional assembly and test into higher-value areas such as advanced test, precision automation, photonics packaging, process infrastructure and chiplet-related design support.

Local OSAT-related names such as Inari, MPI, and Unisem are the more direct proxies. Inari offers exposure to RF and optoelectronics packaging, with longer-term relevance to optical communications and AI networking. MPI, via Carsem, has exposure to automotive, industrial and power-related packaging, while Unisem remains relevant in automotive, industrial and power management applications.

Automation and test equipment players could be among the clearer beneficiaries, given that advanced packaging requires higher precision in die placement, handling, inspection, alignment, bonding and testing. Relevant Malaysian names include Pentamaster, ViTrox, Greatech, Mi Technovation, and Aemulus. Among these, Pentamaster is relevant for semiconductor automation and test handling, ViTrox for machine vision inspection, and Aemulus for semiconductor test solutions.

Precision engineering and process infrastructure players may benefit indirectly from rising advanced packaging capex. UWC, Kobay and SAM Engineering could benefit from demand for precision components and equipment modules, while KGB and Frontken offer exposure to semiconductor facility infrastructure, ultra-high-purity systems, process support and precision cleaning.

Longer term, photonics and chiplet-related opportunities could also emerge. Inari, Pentamaster, ViTrox, NatGate and PIE may be worth monitoring for optical, AI networking or high-speed connectivity exposure, while Oppstar and SkyeChip are relevant to IC design and chiplet/package co-design.

Overall, Malaysia's advanced packaging opportunity should be viewed as an ecosystem theme rather than a broad-based sector uplift. The key beneficiaries are likely to be companies with credible exposure to advanced test, automation, precision engineering, photonics packaging, process infrastructure and higher-complexity semiconductor programmes.

Forming Malaysia Advanced Packaging Consortium (MAPC) to move up the value chain
Malaysia had recently forming Malaysia Advanced Packaging Consortium (MAPC) through collaboration among five local companies (namely, **Skyechip, FusionAP, Inari, Pentamaster, and NSW Automation**) to help upgrade the country's semicondocutor industry into a higher-value sector. The government has approved a RM92m R&D grant over 24 months for the programme, while industry is conributiog RM93m, bringing the total to RM185m. The main objective of the initiative is to strengthen Mlaaysia's position in high-value semiconductor manfacturing, as the country aims to capture 7% of the global advanced packaging market by 2035.

From an investment perspective, the initiative is strategically positive but still early-stage. The near-term impact is likely to be capability-building rather than immediate earnings contribution. However, the read-through is positive for companies with exposure to advanced packaging, ATE, automation, OSAT process development and high-precision engineering. **SkyeChip** provides the IC design starting point, while **Fusion AP** appears to bring advanced packaging technology and process integration capability. **Inari** appears to be the OSAT/production-line anchor, while **Pentamaster** and **NSW Automation** are positioned as key equipment/test/automation enablers. MAPC believes Malaysia's attractiveness as an advanced packaging base, citing the country's experienced semiconductor talent pool, long-established industry-government collaboration and existing ecosystem as key reasons for locating the business in Malaysia.

MAPC has laid out a phased roadmap to build Malaysia's advanced packaging capability. In 2026, the focus is on early engineering and pilot validation, with Fusion AP working with SkyeChip, and Inari's SiP/flip-chip BGA lines to develop the first demonstrator part.

By 2027, MAPC aims to establish a C4 bumping line in Malaysia. While not a new technology, C4 bumping remains a key interconnect process for flip-chip and advanced packaging, supporting higher-value applications in AI, data centres, networking, automotive and advanced consumer electronics. Note that, C4 bumping is a key enabling process for flip-chip packaging, providing high-density electrical connections between the die and the package substrate. It supports better electrical performance, shorter signal paths, improved I/O density and better thermal handling versus wire bonding.

By 2028, MAPC plans to move into 2.5D die-on-silicon-substrate/interposer packaging, positioning Malaysia closer to next-generation AI and high-performance computing packaging. Longer term, MAPC is also looking at co-packaged optics, optical chip integration and finer-pitch interconnects, potentially scaling from today's 30–40 micron range towards 10 microns before hybrid bonding becomes necessary.

Overall, the roadmap suggests a gradual move from engineering services and pilot-line validation in 2026, to C4 bumping in 2027, and 2.5D advanced packaging capability by 2028, supporting Malaysia's ambition to move beyond conventional backend assembly into higher-value semiconductor packaging.

Exhibit 15: MAPC MOU

Source: MAPC, Kenanga Research

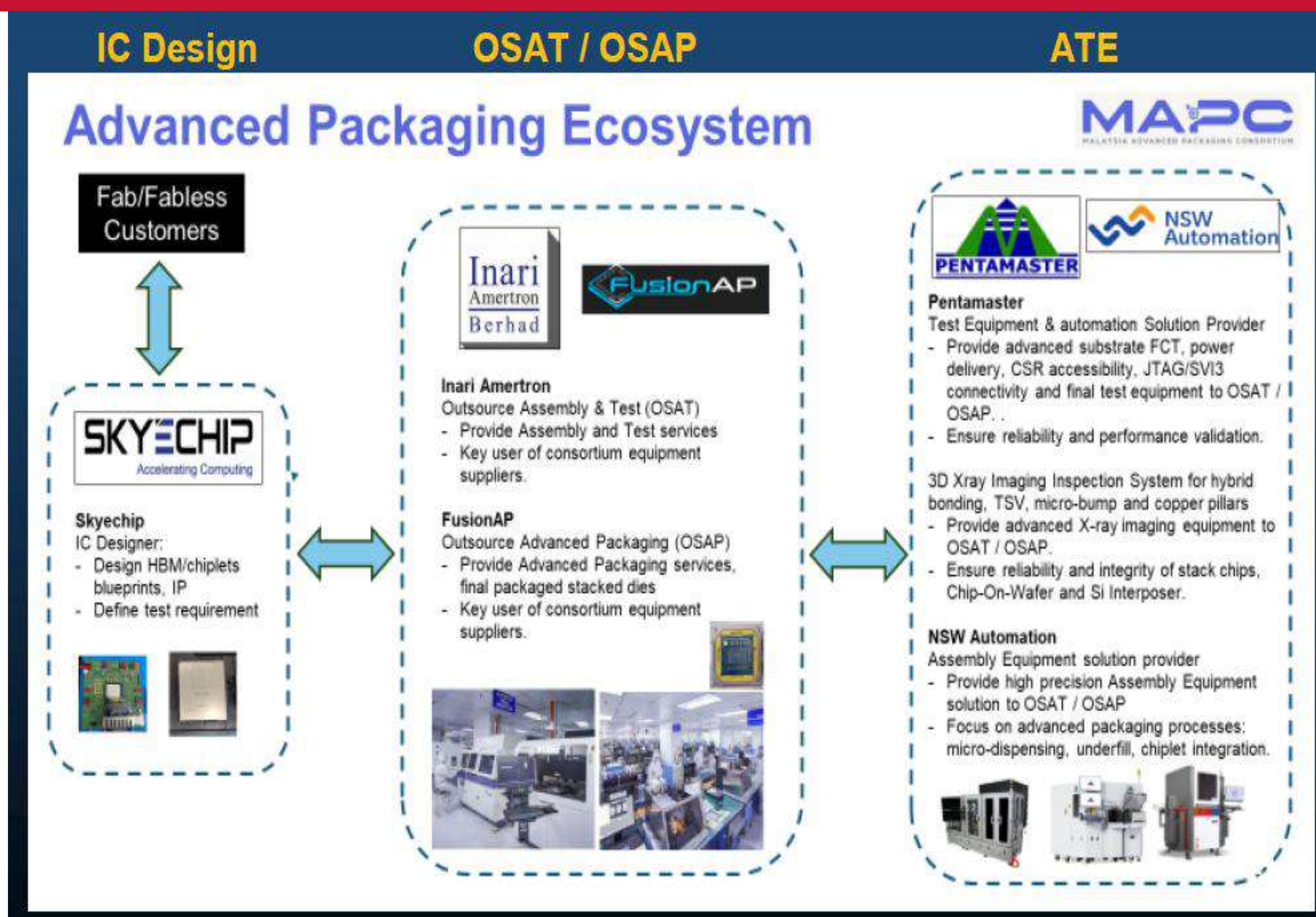
Exhibit 16: MAPC Signing Ceremony

Source: MAPC, Kenanga Research

Exhibit 17: MAPC – Advanced Packaging is a New Capability

Source: MAPC, Kenanga Research

Exhibit 18: Roles of Each Founding Member



Source: MAPC, Kenanga Research

Stay selective after the strong rally

Overall, we continue to remain constructive on the technology sector's medium-to-longer term outlook, underpinned by resilient AI infrastructure spending and continued global fab expansion. SEMI expects global installed capacity to grow by 4.7%–5.0% in 2026, and for front-end equipment spending to hit a record USD133b (+18% YoY), signalling a shift from fab construction in 2025 towards equipment installation and capacity ramp-up in 2026. Meanwhile, capex guidance by Magnificent 7 now adds up to roughly USD720b–USD750b, reinforcing demand visibility for AI-related beneficiaries. However, after the sharp rally in both SOX and KLTEC, we believe short-term mean-reversion risk has increased, especially amid higher bond yields, potential liquidity absorption from mega tech IPOs, Fed policy uncertainty and stronger US labour data, which could dampen hopes of near-term rate cuts. Hence, we advocate trimming trading positions and locking in partial gains, while maintaining core exposure to fundamentally strong names. We maintained our NEUTRAL call for the sector and continue to favour KGB (OP, TP: RM9.05), UWC (OP, TP: 4.70), FRONTKN (OP, TP: RM5.10) and INFOMINA (OP, TP: RM1.90) as our top pick for the sector due to their stronger order visibility, margin resilience and AI/front-end exposure, while staying cautious on EMS names given weak end-demand and FX sensitivity. Overall, we remain positive on the structural AI cycle, but believe investors should turn more selective and disciplined after the recent strong rally *(please refer to 8 June tech sector report (title: Time to Lock in Some Gains, not Exit the Theme) for details).*

Malaysian Technology Peers Comparison

Name	Rating	Last Price @ 12 Jun (RM)	Target Price (RM)	Upside	Mkt Cap (RM m)	Shariah Compliant	Current FYE	Core EPS (sen)		Core EPS Growth		PER (x) – Core Earnings		PBV (x)	ROE	Net. Div. (sen)	Net. Div. Yld
								1-Yr. Fwd.	2-Yr. Fwd.	1-Yr. Fwd.	2-Yr. Fwd.	1-Yr. Fwd.	2-Yr. Fwd.	1-Yr. Fwd.	1-Yr. Fwd.	1-Yr. Fwd.	1-Yr. Fwd.
D&O GREEN TECHNOLOGIES BHD	MP	0.395	0.440	11.4%	489.6	Y	12/2026	(2.6)	2.0	-385.8%	-0.3%	N.A.	19.8	0.9	-16.6%	1.0	2.5%
FRONTKEN BHD	OP	4.75	5.10	7.4%	8,611.4	Y	12/2026	12.8	13.9	31.9%	8.7%	37.2	34.2	6.6	19.1%	4.0	0.8%
INARI AMERTRON BHD	OP	2.16	2.42	12.0%	8,240.8	Y	06/2026	4.8	8.0	-28.1%	64.6%	44.7	27.2	3.0	5.9%	5.0	2.3%
KELINGTON GROUP BHD	OP	7.71	9.05	17.4%	6,659.7	Y	12/2026	21.4	24.5	29.1%	14.1%	36.0	31.5	8.7	27.5%	15.0	1.9%
LGMS BHD	OP	0.470	0.580	23.4%	214.3	Y	12/2026	2.9	3.6	30.4%	21.8%	16.1	13.2	1.6	10.5%	2.0	4.3%
M'SIAN PACIFIC INDUSTRIES BHD	MP	47.50	38.90	-18.1%	9,471.4	Y	06/2026	104.7	134.1	35.6%	28.0%	45.4	35.4	4.3	9.7%	40.0	0.8%
NATIONGATE HOLDINGS BHD	MP	0.760	0.780	2.6%	1,719.6	Y	12/2026	3.5	5.2	-20.1%	49.3%	21.8	14.6	1.6	7.6%	2.0	2.6%
OPPSTAR BHD	UP	0.530	0.430	-18.9%	341.0	Y	03/2027	1.2	2.0	-50.9%	58.2%	43.0	27.2	2.6	6.3%	0.0	0.0%
P.I.E. INDUSTRIAL BHD	MP	1.57	1.45	-7.6%	602.9	Y	12/2026	5.9	8.4	0.4%	42.3%	26.6	18.7	0.9	3.5%	0.0	0.0%
SKP RESOURCES BHD	UP	0.330	0.300	-9.1%	515.6	Y	03/2027	2.5	3.5	-19.4%	42.0%	13.4	9.4	0.5	3.7%	0.0	0.0%
SKYECHIP BHD	OP	2.84	2.00	-29.6%	5,100.6	Y	03/2027	2.6	3.4	30.1%	32.1%	109.2	82.7	29.4	31.2%	70.0	24.6%
UNISEM (M) BHD	UP	4.60	2.47	-46.3%	7,420.2	Y	12/2026	5.4	9.5	39.6%	74.6%	84.5	48.4	3.4	4.1%	0.0	0.0%
UWC BHD	OP	5.60	4.70	-16.1%	6,178.6	Y	07/2026	9.0	14.3	143.3%	59.0%	62.5	39.3	10.7	18.7%	0.0	0.0%
PENTAMASTER CORP BHD	MP	4.31	3.95	-8.4%	3,065.8	Y	12/2026	12.1	13.1	39.0%	8.1%	35.6	32.9	3.6	10.4%	2.0	0.5%
INFOMINA BHD	OP	1.09	1.90	74.3%	655.4	Y	05/2026	5.6	7.6	60.7%	34.8%	19.3	14.3	3.3	18.3%	1.0	0.9%
Simple Average					**59,287.0**					**14.6%**	**40.4%**	**46.3**	**33.0**	**5.4**	**10.7%**		**2.8%**

Source: Kenanga Research

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Stock Ratings are defined as follows:

Stock Recommendations

OUTPERFORM : A particular stock's Expected Total Return is MORE than 10%
MARKET PERFORM : A particular stock's Expected Total Return is WITHIN the range of -5% to 10%
UNDERPERFORM : A particular stock's Expected Total Return is LESS than -5%

Sector Recommendations***

OVERWEIGHT : A particular sector's Expected Total Return is MORE than 10%
NEUTRAL : A particular sector's Expected Total Return is WITHIN the range of -5% to 10%
UNDERWEIGHT : A particular sector's Expected Total Return is LESS than -5%

Sector recommendations are defined based on market capitalisation weighted average expected total return for stocks under our coverage.

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